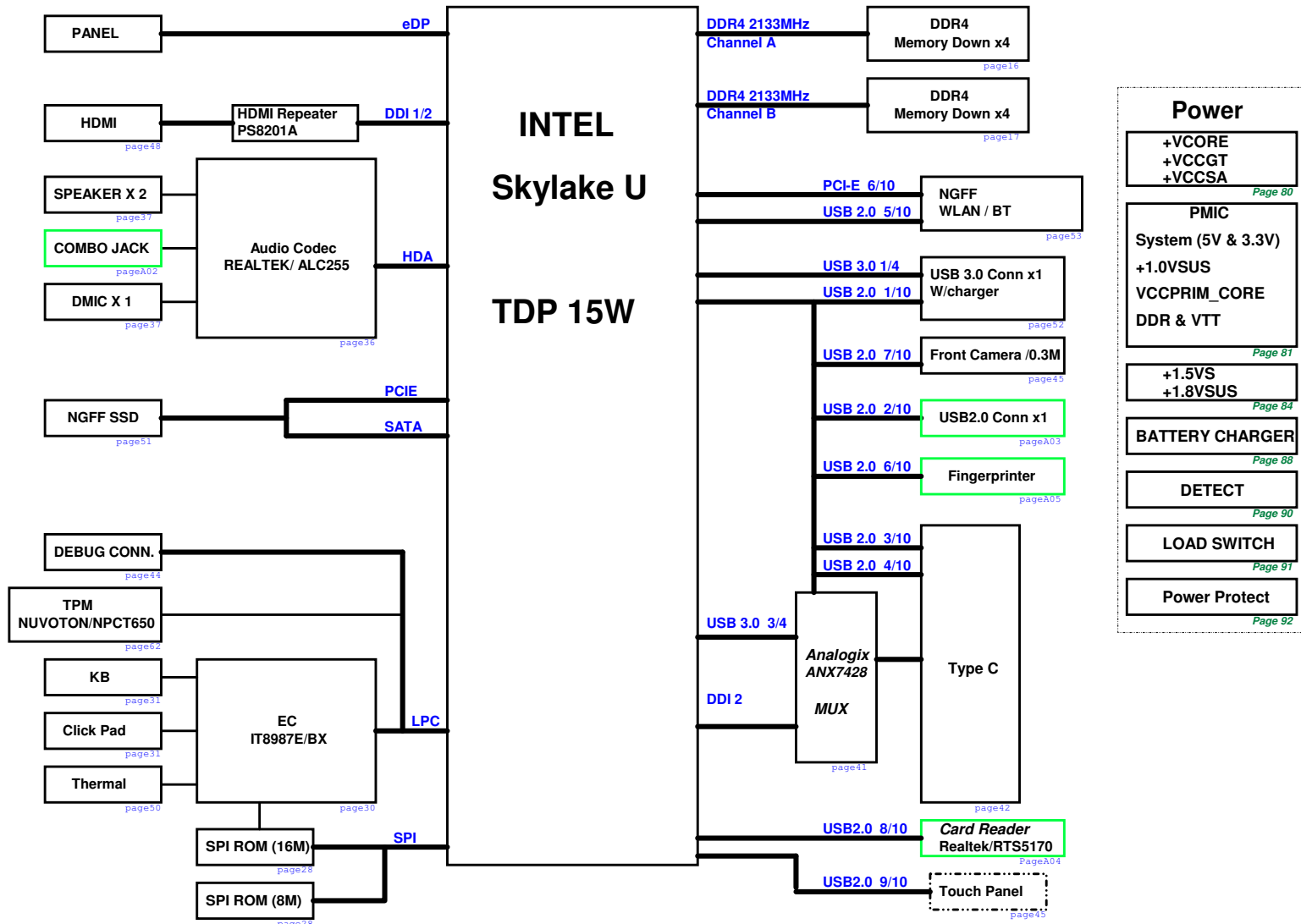


# 14" Cassiopeia (X3) for Skylake U Platform Block Diagram



Discharge Circuit

Page 57

DC &amp; BATT. Conn.

Page 60

Reset Circuit

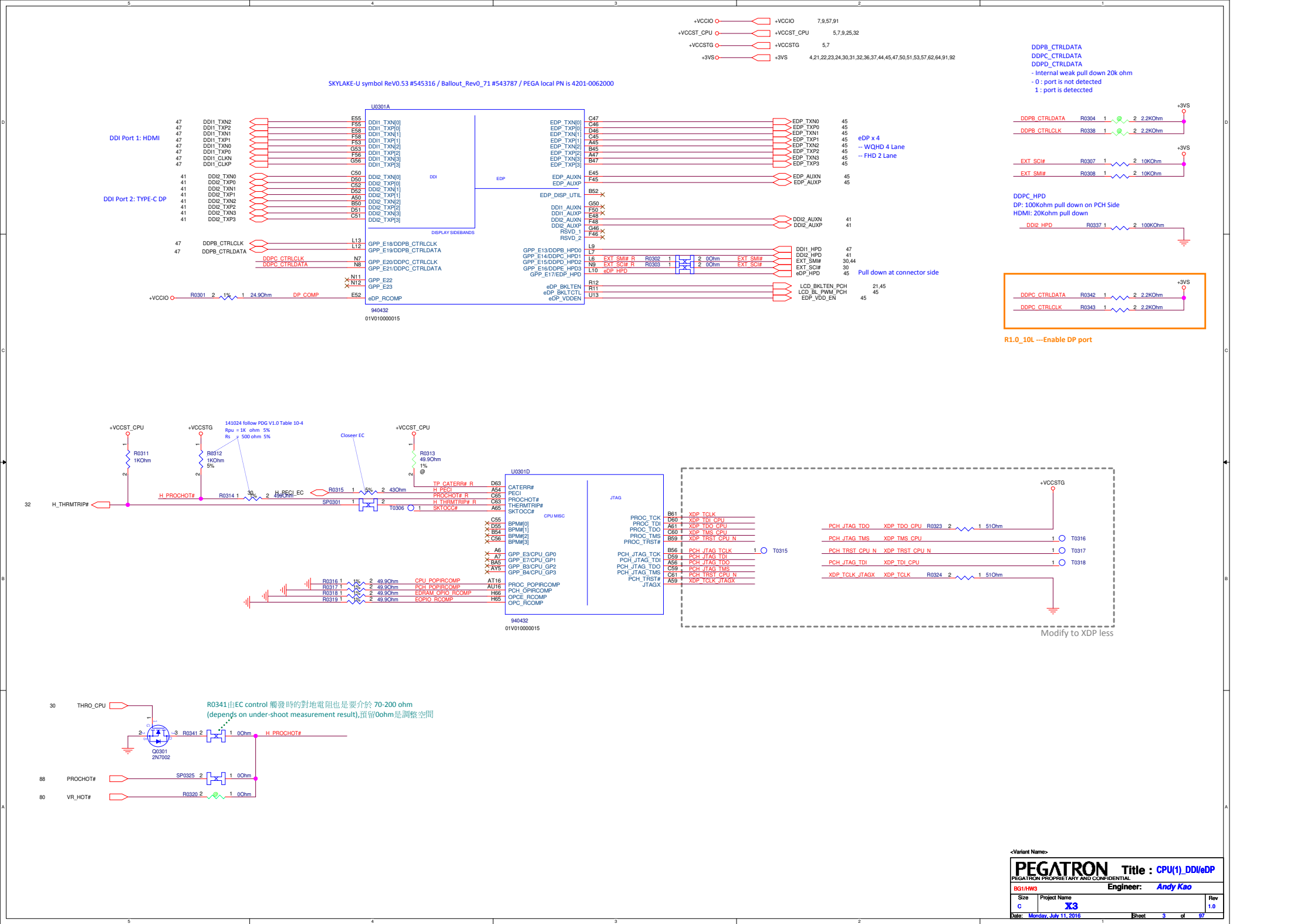
Page 32

Skew Holes

Page 65

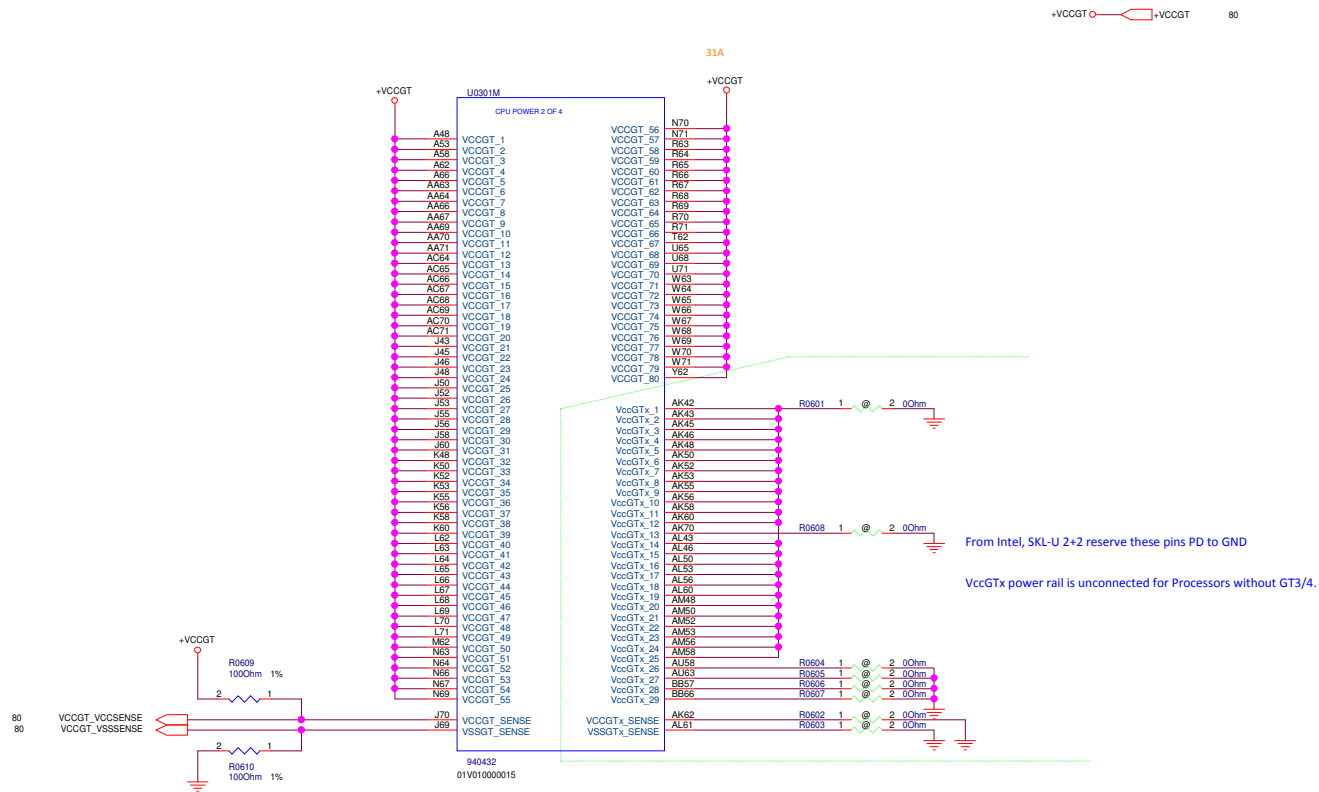
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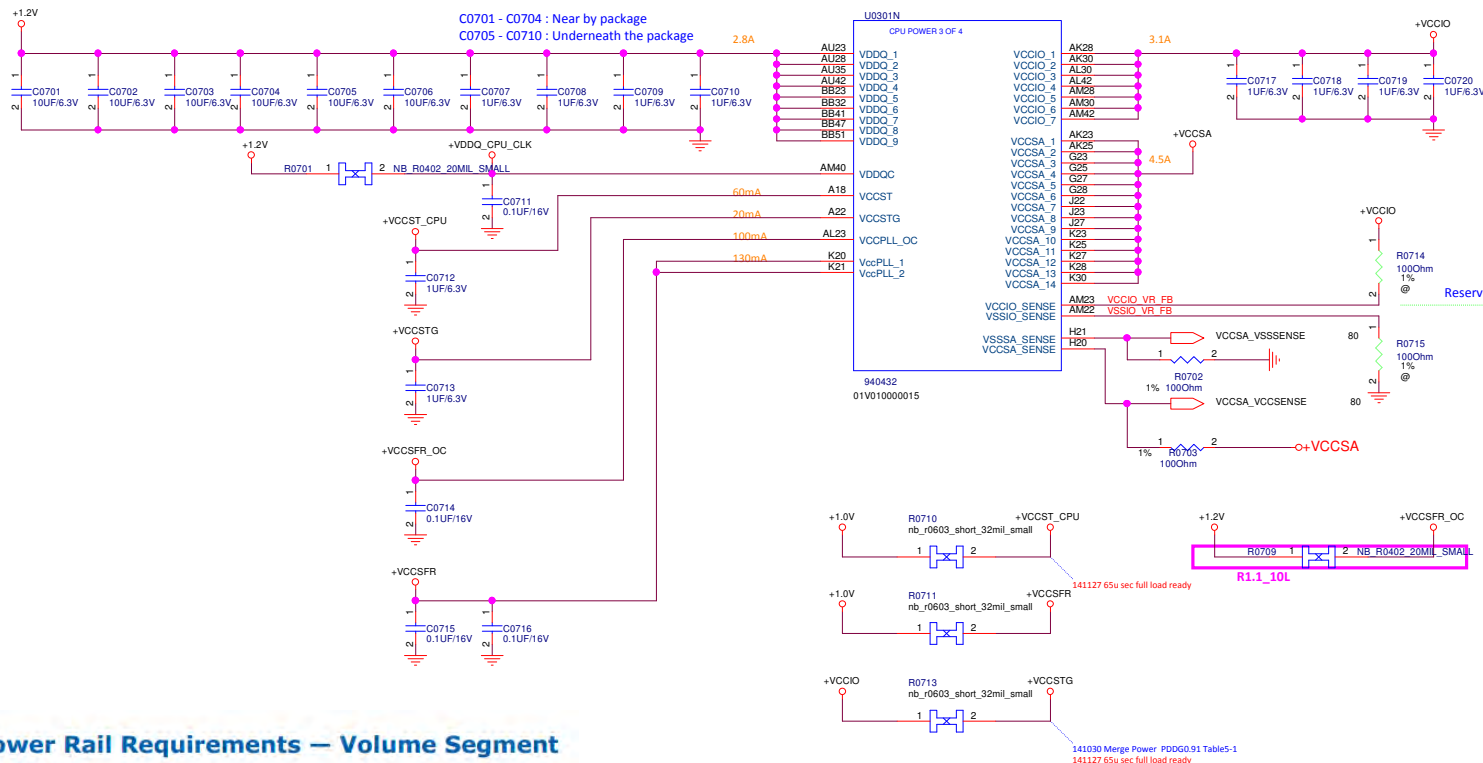








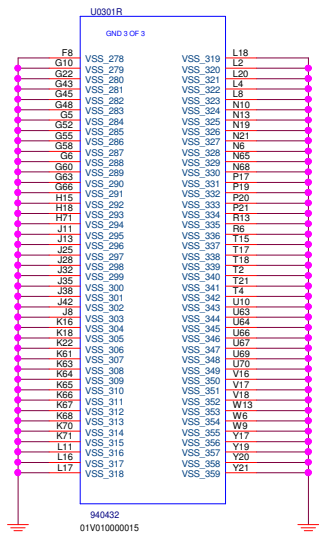
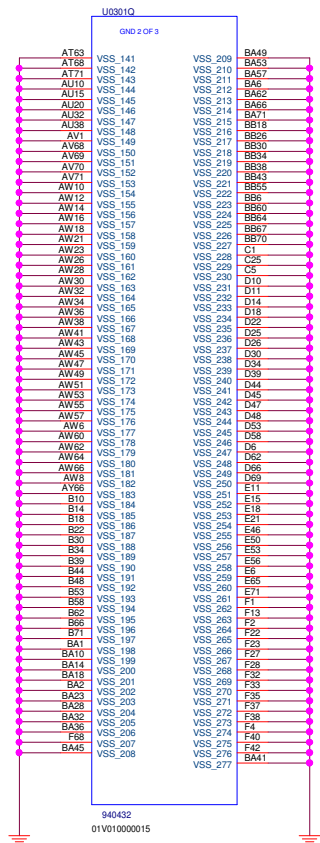
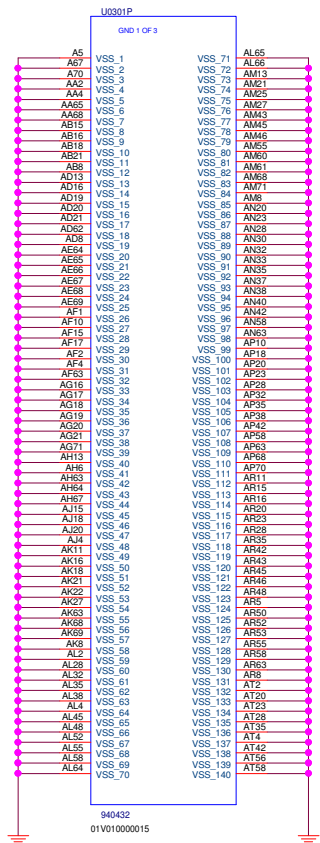




**Table 5-1. Power Rail Requirements — Volume Segment — U-Line**

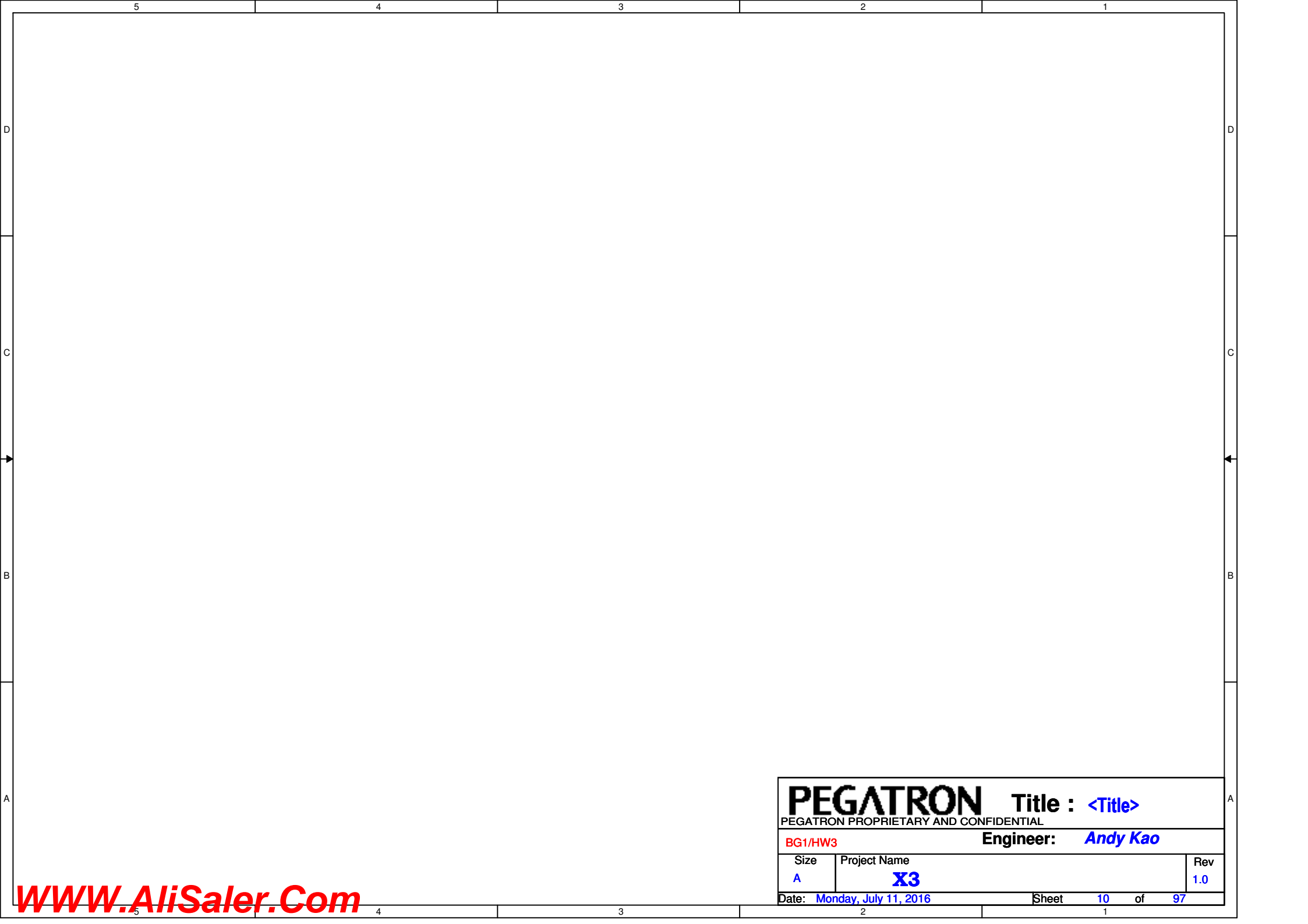
Load switch (LS)	LS ENABLE	Load/Rail name	I <sub>max</sub> (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc <sub>ST</sub>	0.04
		Vcc <sub>PLL</sub> (Vcc <sub>SFR</sub> )	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	Vcc <sub>IO</sub>	3.0
		Vcc <sub>STG</sub>	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu\_04

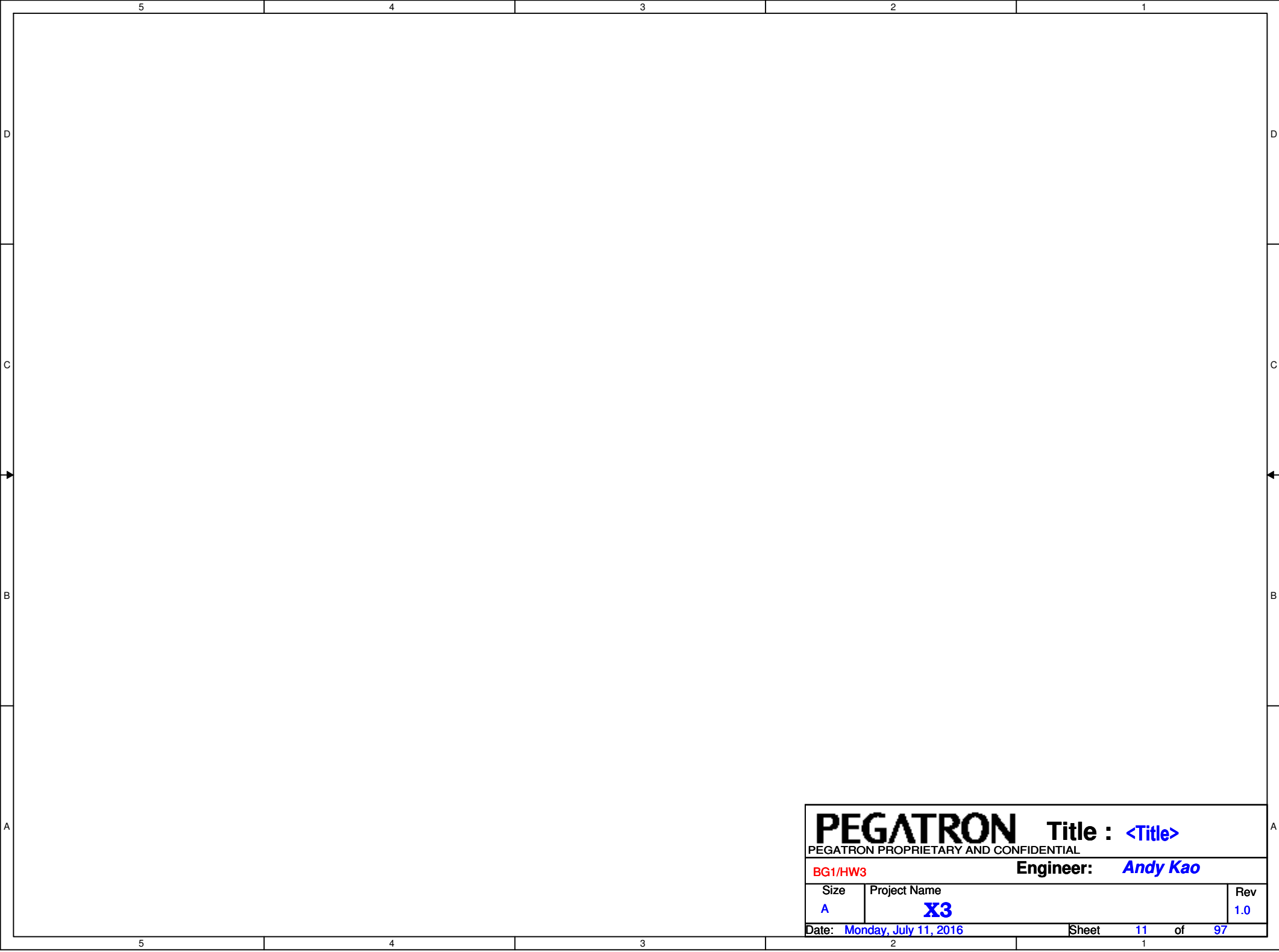




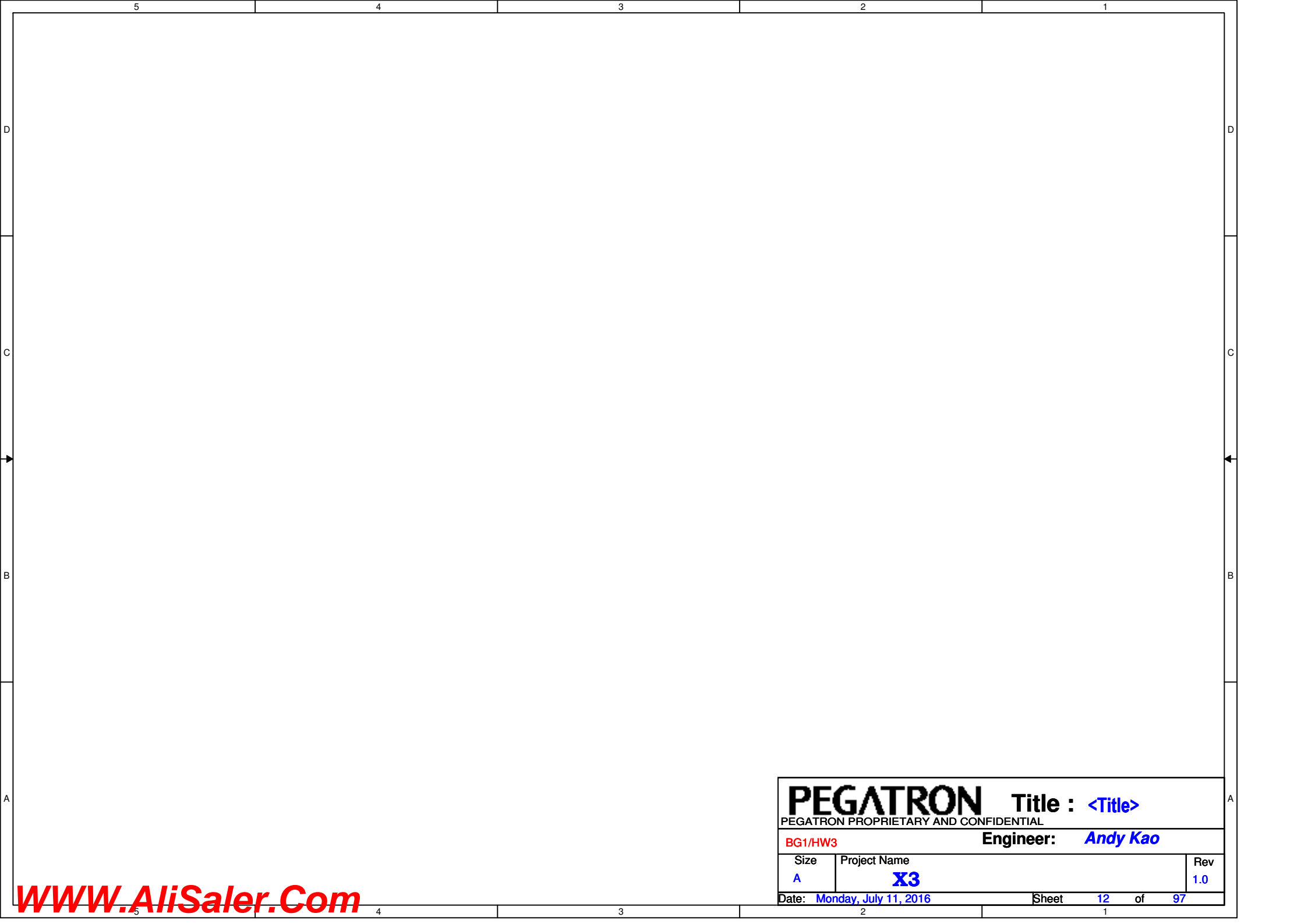




<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	10 of 97

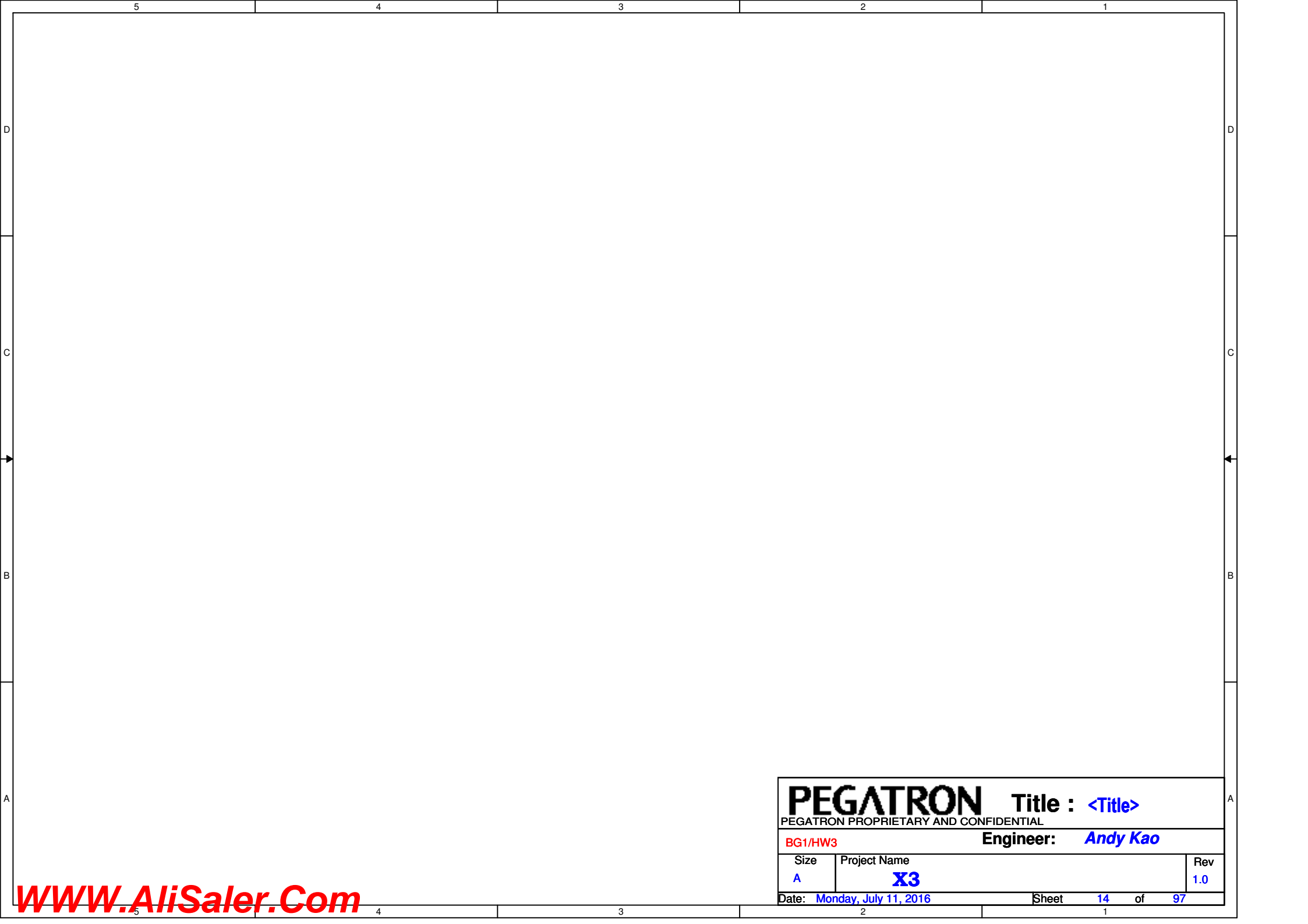


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>11</b> of <b>97</b>





<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	12 of 97

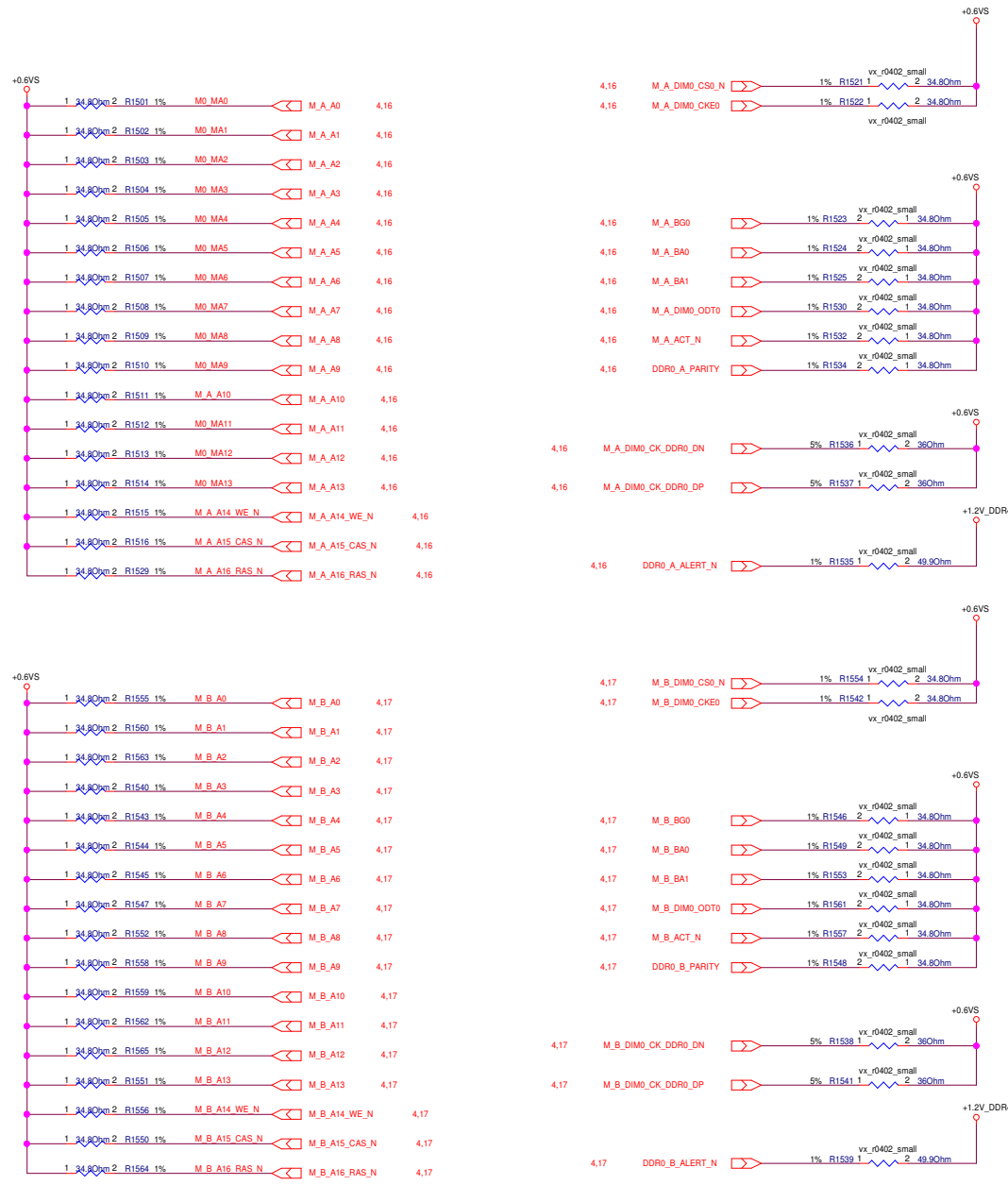
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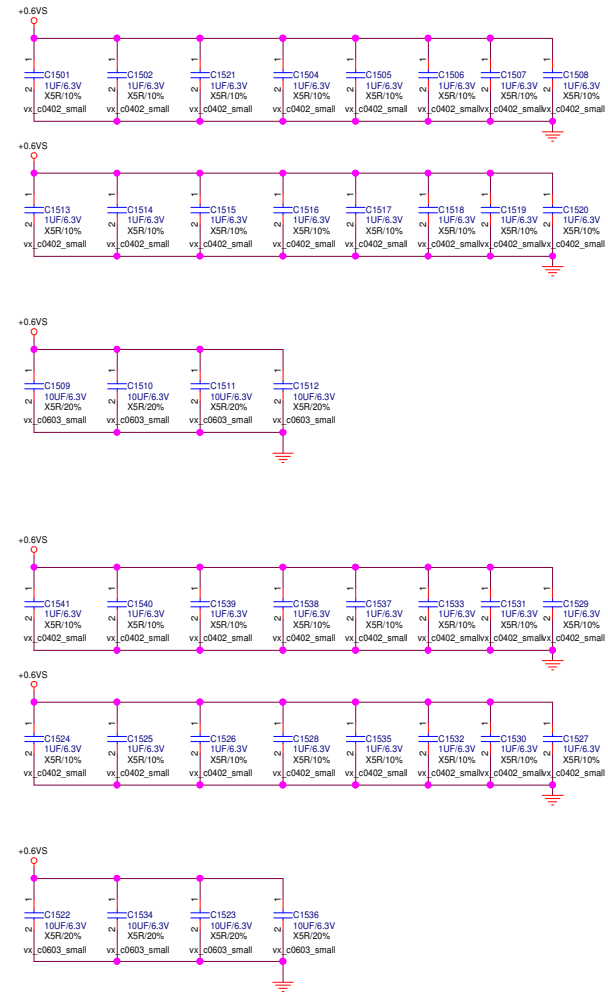
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BG1/HW3			Engineer: Andy Kao		
Size	Project Name				Rev
A	X3				1.0
Date: Monday, July 11, 2016			Sheet	14	of 97

# DDR4(0)\_Termination

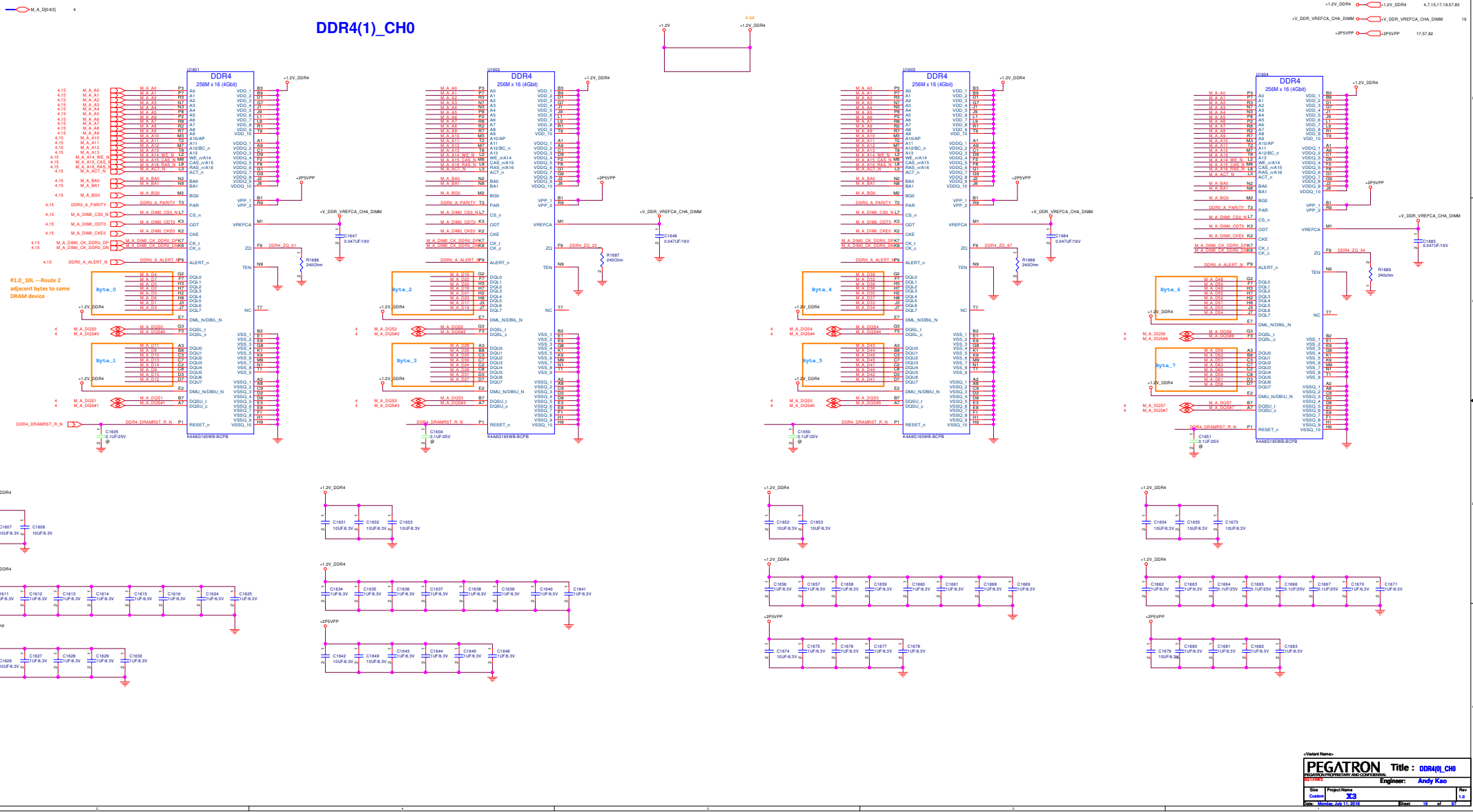
+0.6VS  +0.6VS 57,83  
+1.2V\_DDR4  +1.2V\_DDR4 4,7,16,17,19,57,83



Average placed close to +VDDQ\_VTT power plane

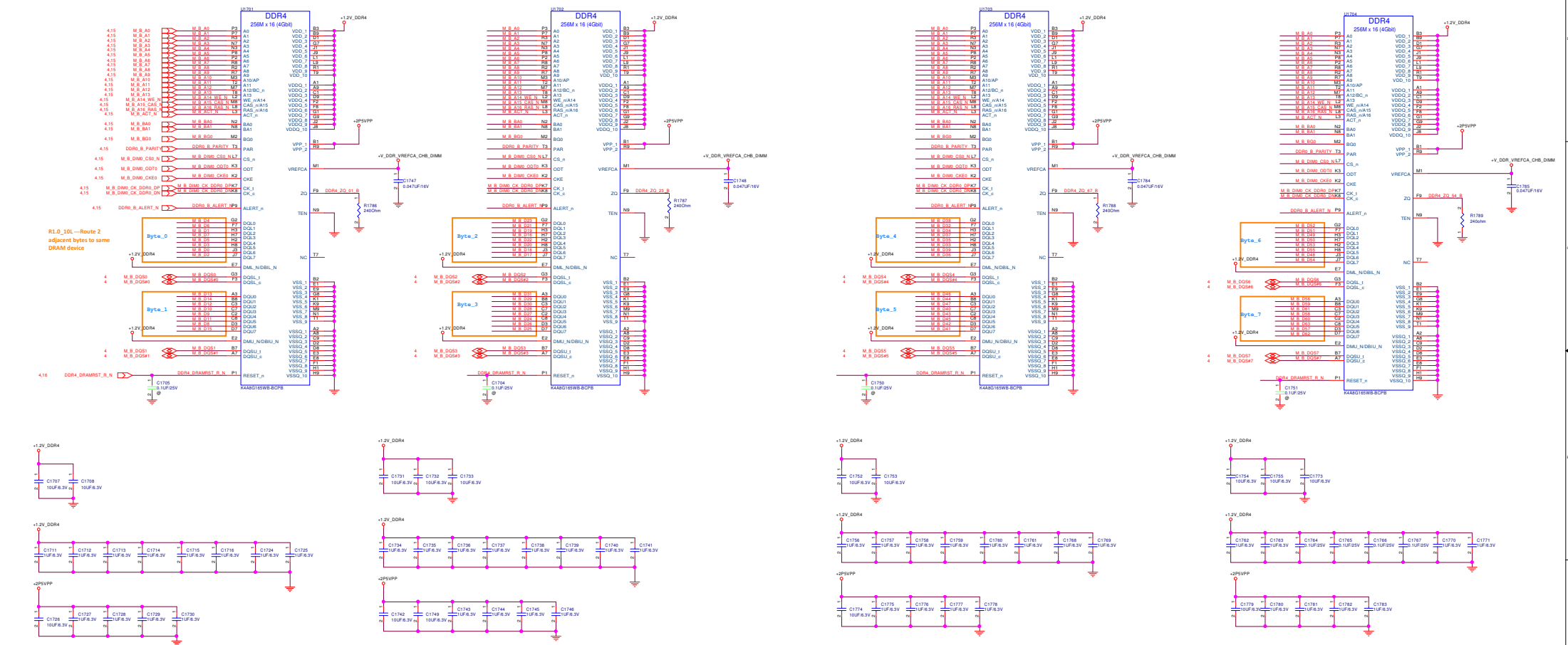


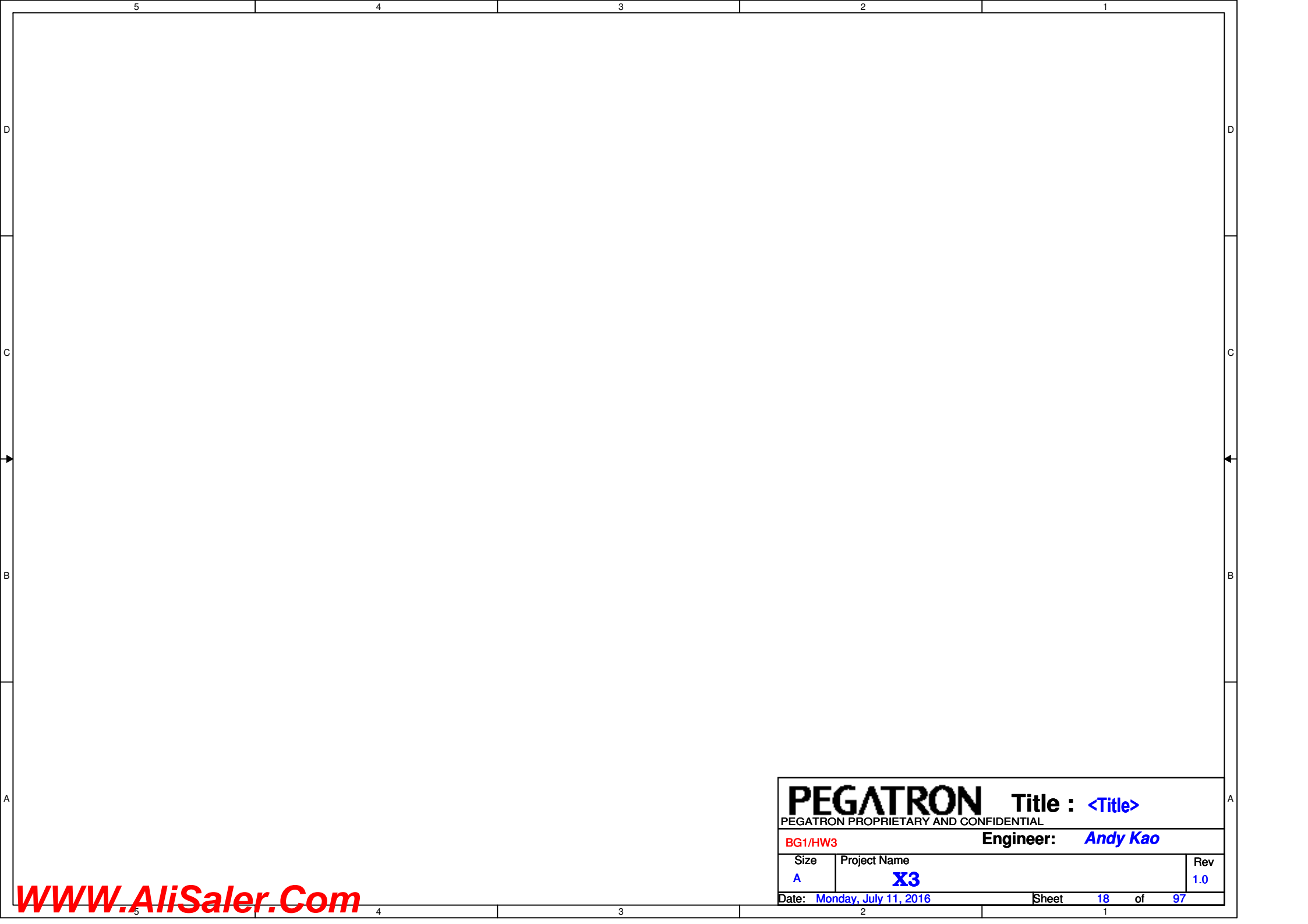
DDR4(1)\_CH0





DDR4(2)\_CH1



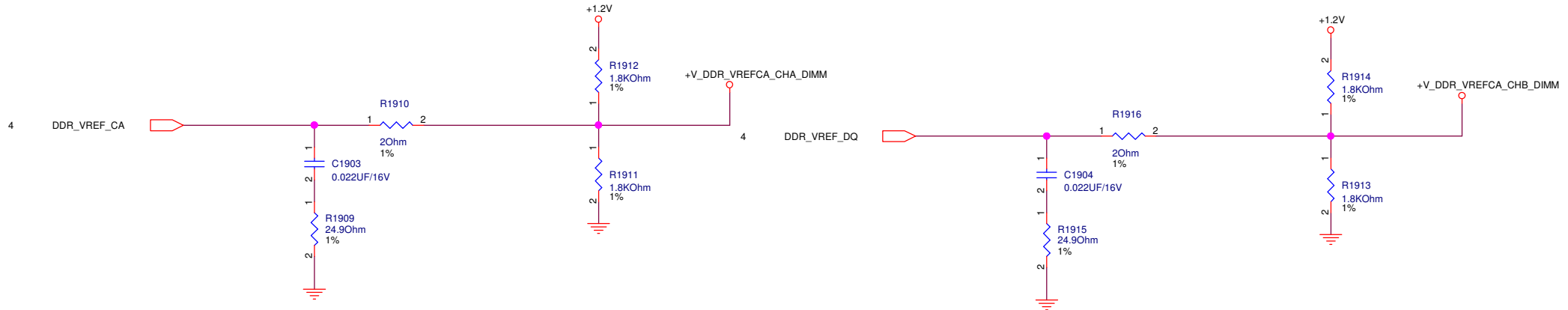


<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	18 of 97

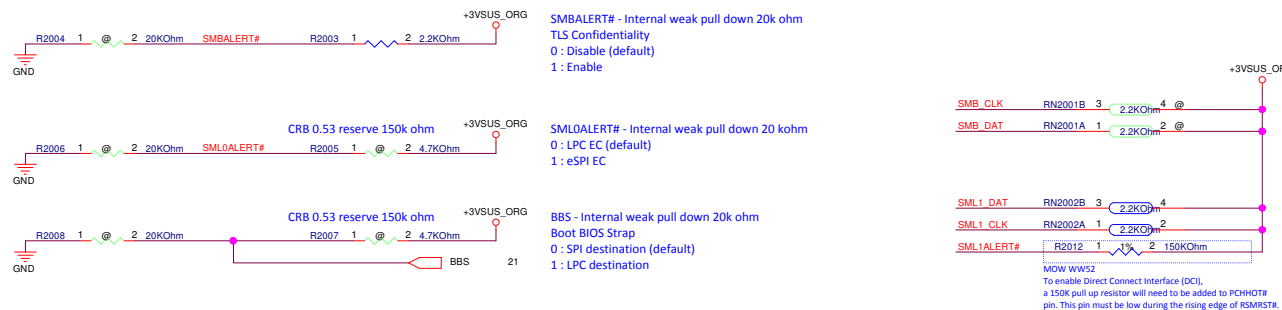
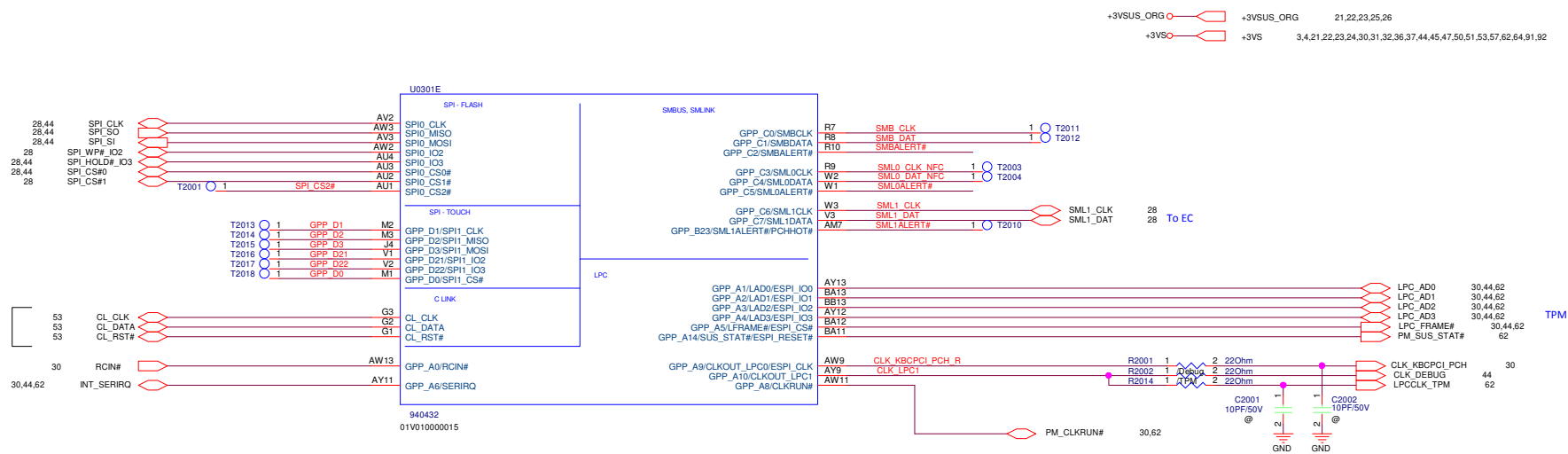
# DDR4(3)\_CA/DQ Voltage

+1.2V		+1.2V	4,7,15,16,17,57,83	
+V_DDR_VREFCA_CHB_DIMM		+V_DDR_VREFCA_CHB_DIMM		17
+V_DDR_VREFCA_CHA_DIMM		+V_DDR_VREFCA_CHA_DIMM		16

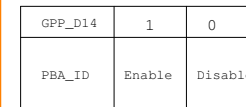
## DDR4 Vref (Intel Schematic Review)



<Variant Name>		
<b>PEGATRON</b> Title : <b>DDR3(3)_CA/DQ Voltage</b>		
BG1/HW3 Engineer: <b>Andy Kao</b>		
Size B	Project Name <b>X3</b>	Rev 1.0
Date: <b>Monday, July 11, 2016</b>	Sheet <b>19</b> of <b>97</b>	



With skylake EHCI Removal, Potential Gap with Windows\* 7 Kernel Debug and OS Installation – Mitigation Required



MB version

PCB\_ID2  
(GPP\_C15)

0

1

---

1

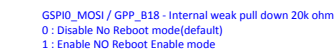
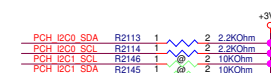
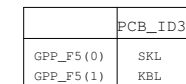
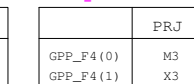
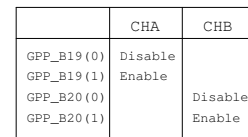
MEM_ID2	MEM_IDC
(GPP B17)	(GPP B19)

0 0

0	1
1	0

1	1
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Default is GPO, to reserve pull high to +3VSUS\_ORG

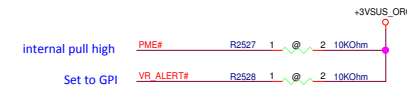
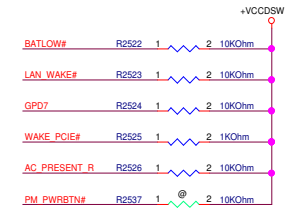
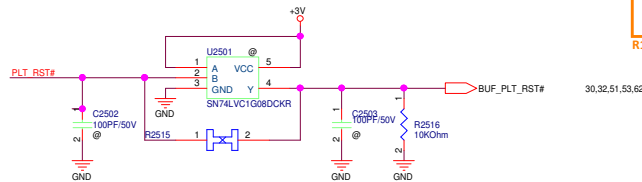
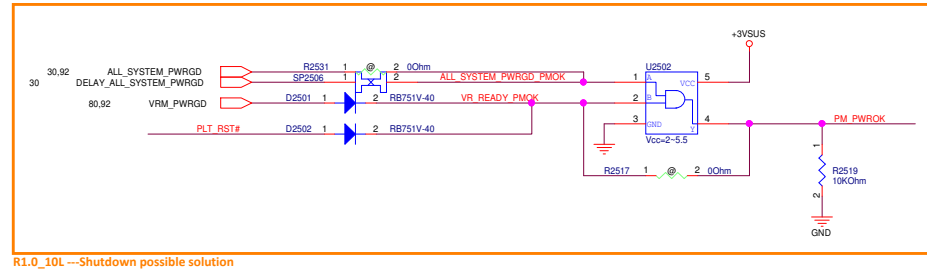
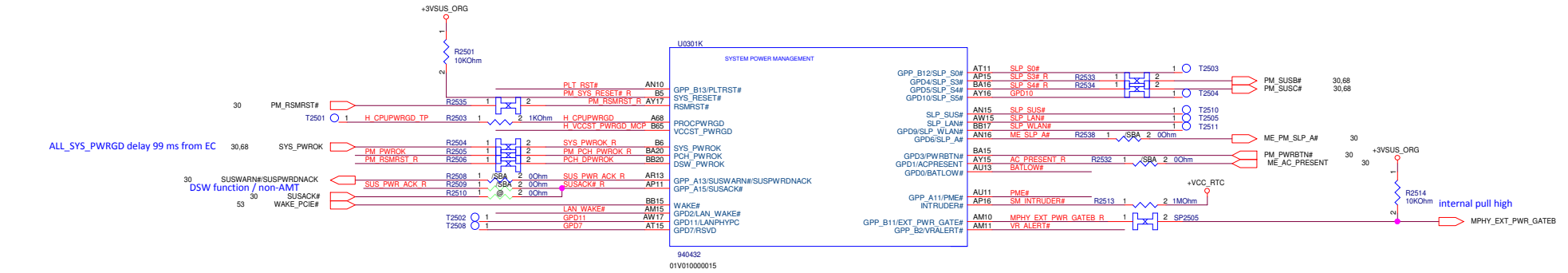


BG1/HW3		Engineer: <b>Andy Kao</b>	
Size <b>C</b>	Project Name <b>X3</b>	Rev <b>1.0</b>	
Date: <b>Monday, July 11, 2016</b>		Sheet <b>23</b> of <b>97</b>	

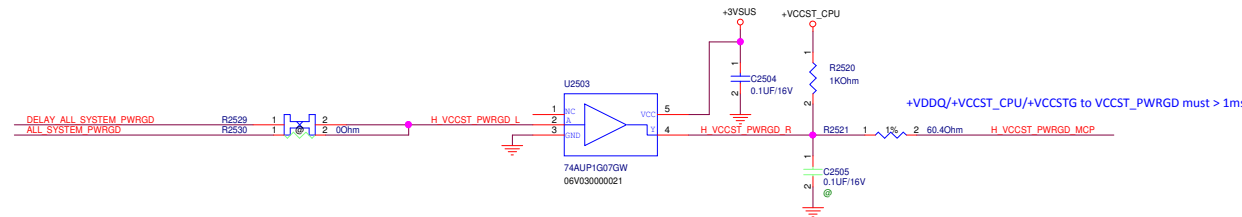




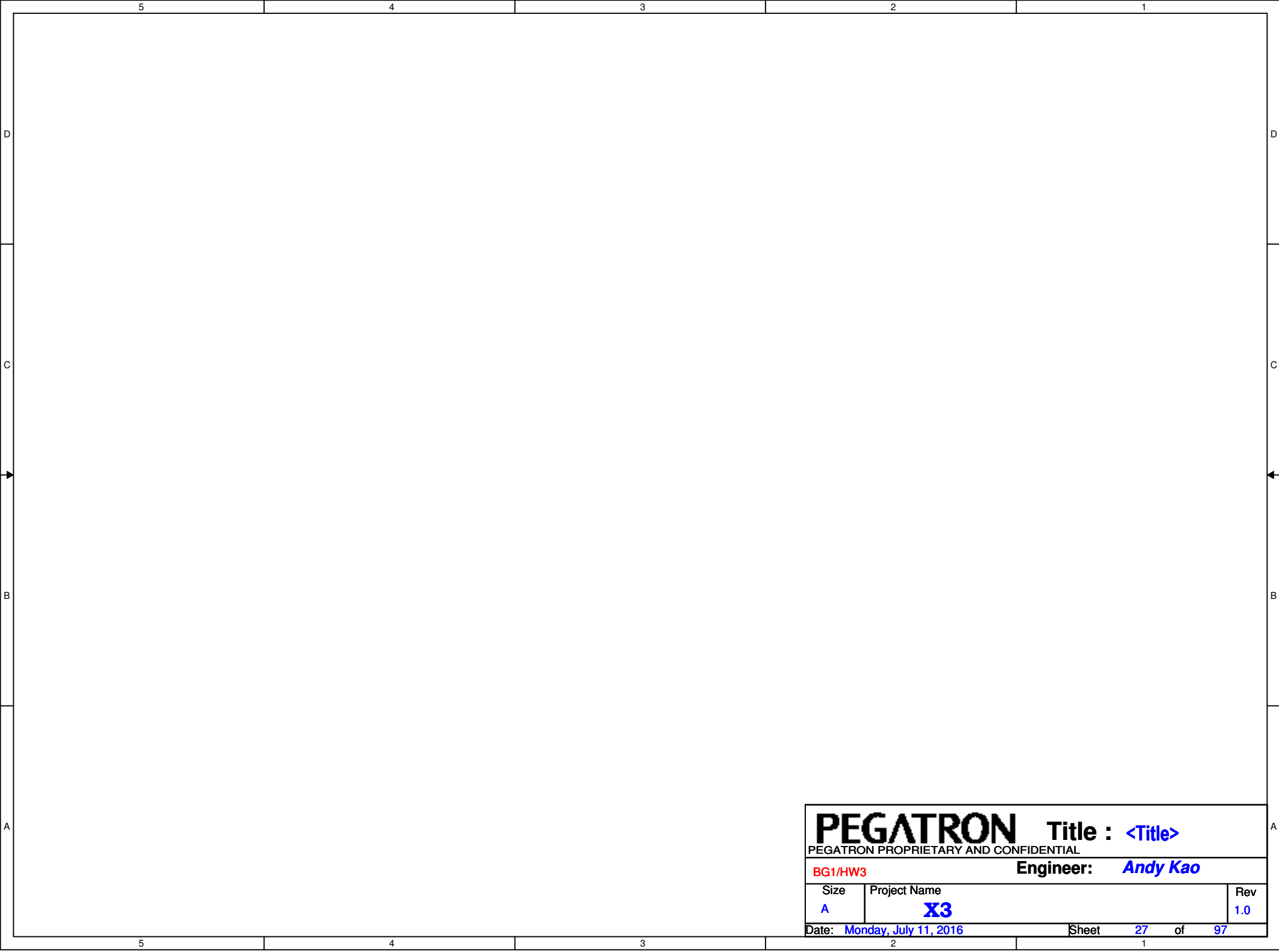
+3VSUS_ORG		+3VSUS_ORG	20,21,22,23,26
+VCC_RTC		+VCC_RTC	24,26,36,60
+VCCDSW		+VCCDSW	26,30
+VCCST_CPU		+VCCST_CPU	3,5,7,9,32
+3V		+3V	31,57,82,91
+3VSUS		+3VSUS	4,24,26,28,30,31,41,42,51,53,62,64,68,81,92



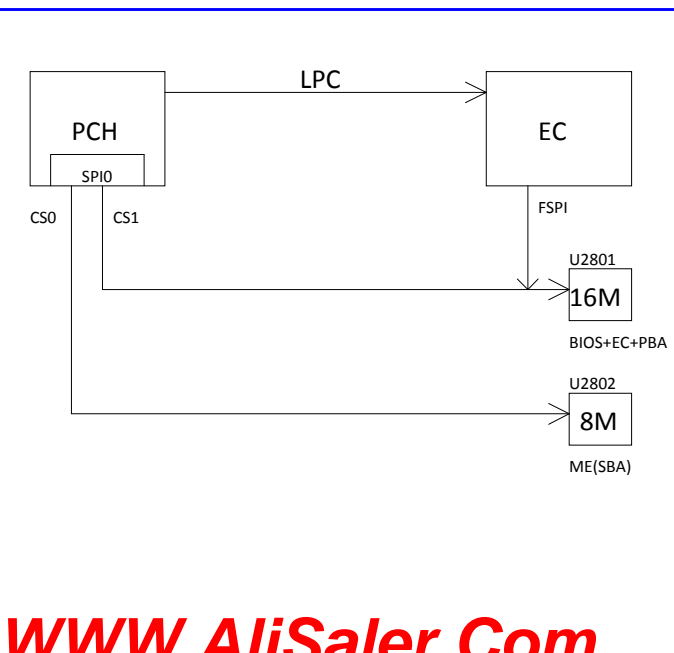
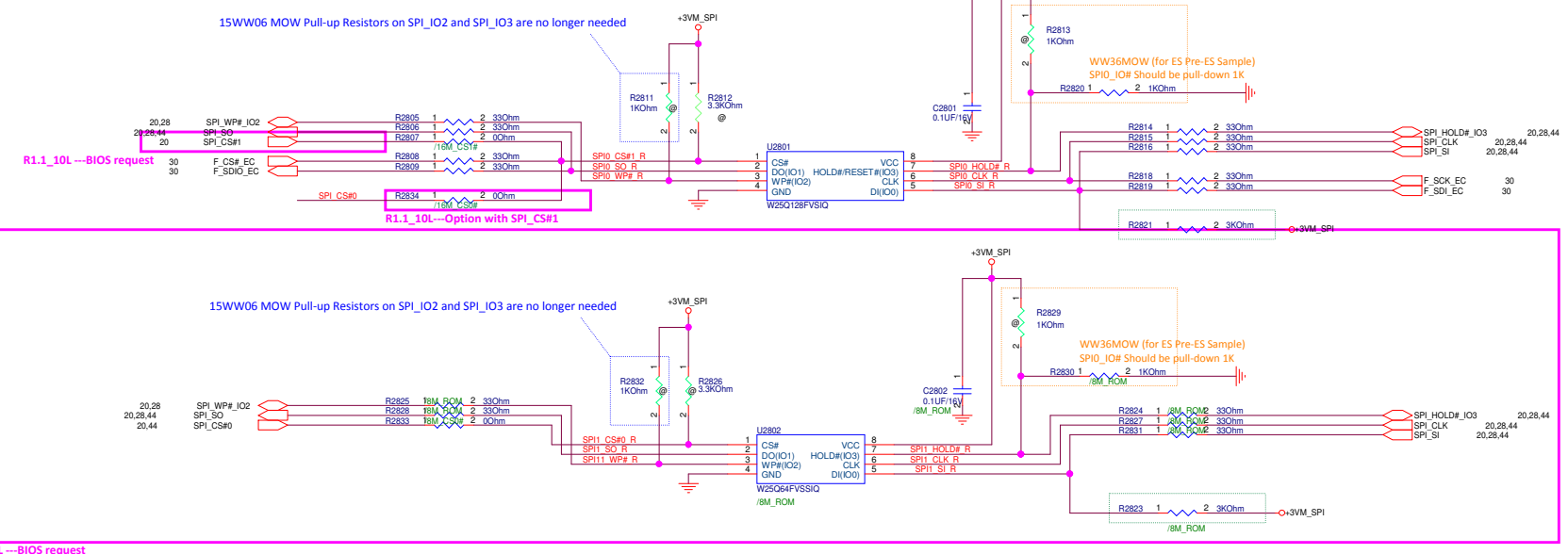
EC delay ALL\_SYSTEM\_PWRGD 2ms



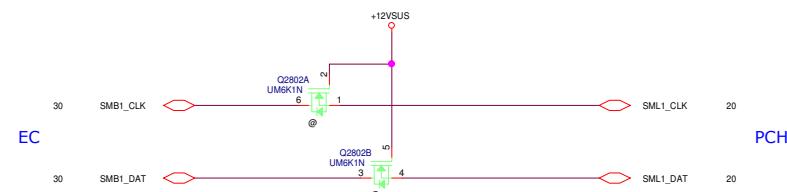




<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <i>X3</i>		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>27</i> of <i>97</i>	



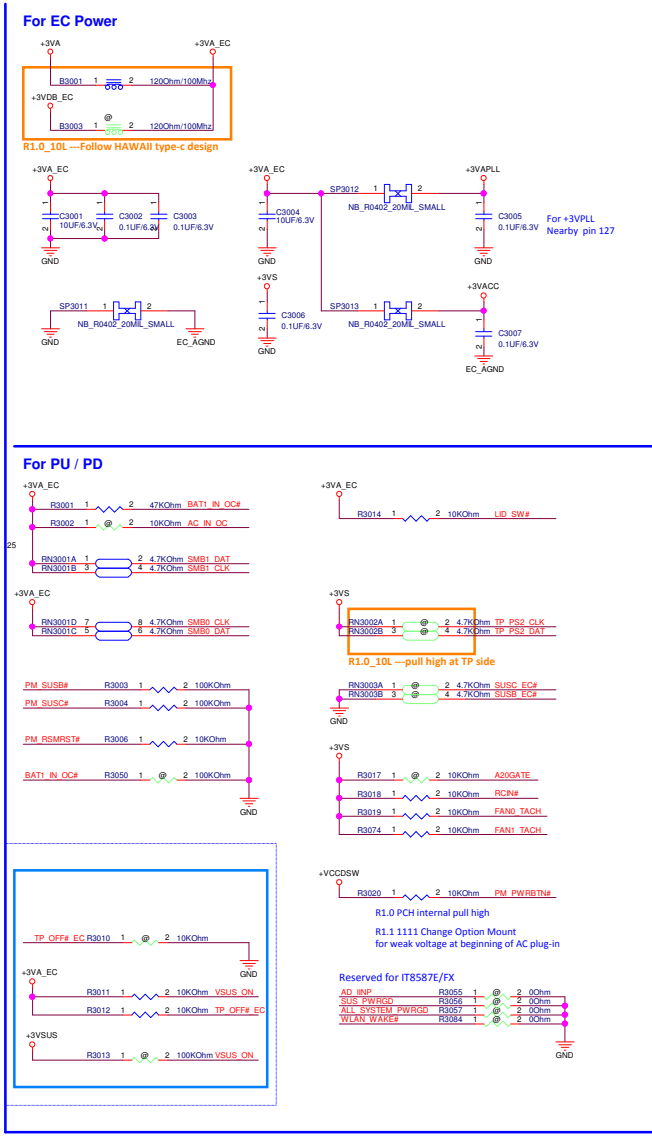
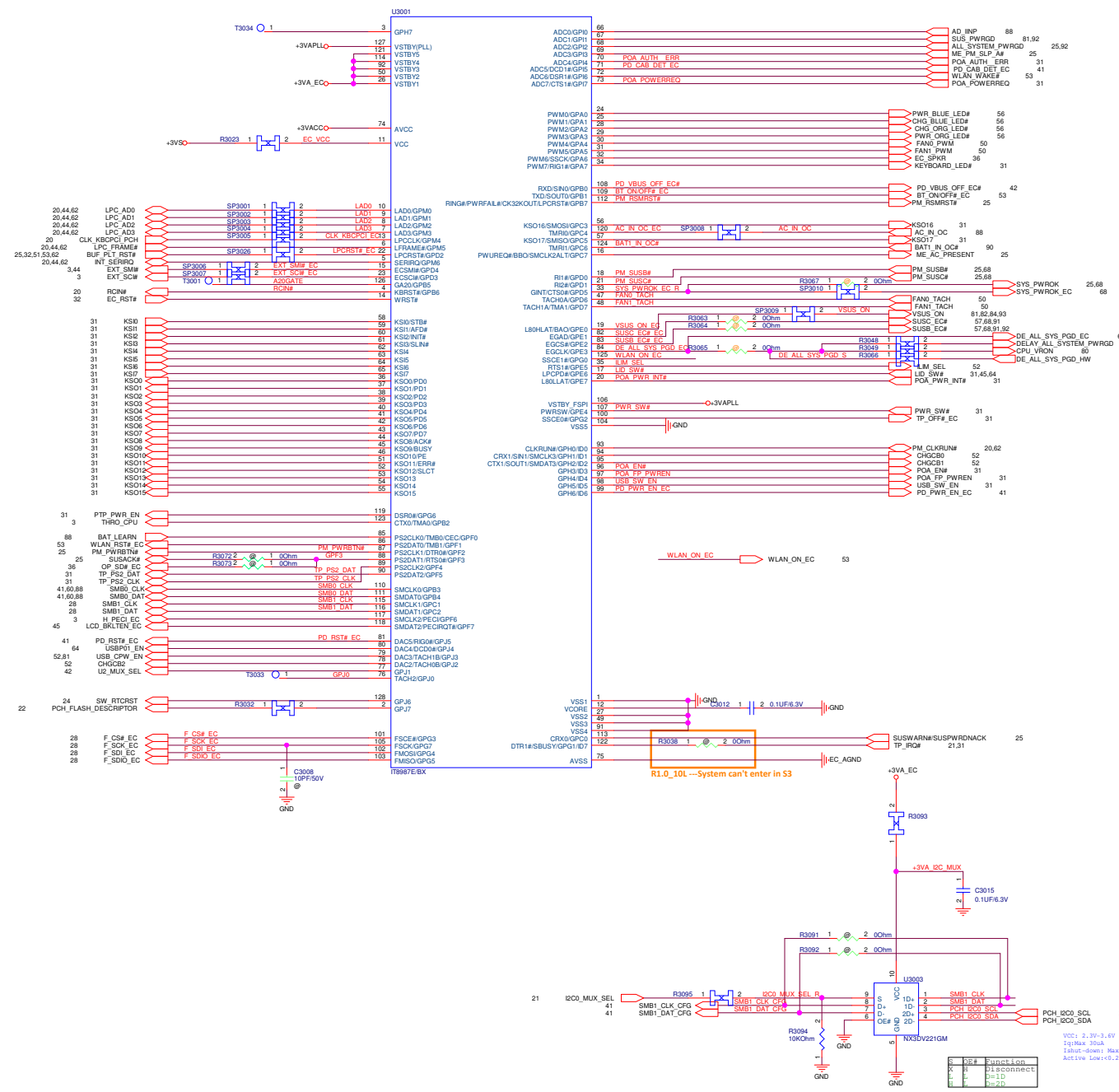
### PCH SMBus



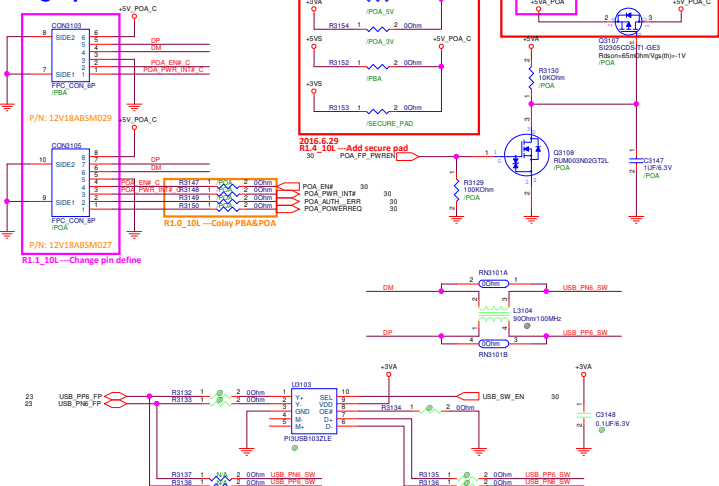
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Pegatron Proprietary and Confidential		
BG1/HW3	Engineer: Andy Kao	
Size	Project Name	Rev
C	X3	1.0
Date: Monday, July 11, 2016	Sheet	26 of 97

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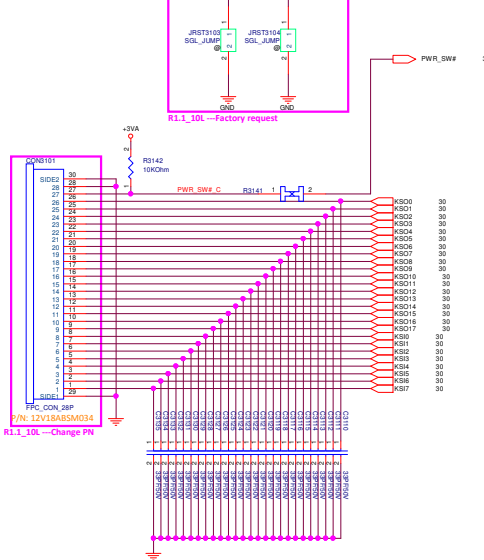
3VA\_EC 28.32,44  
+3VS 3.4,21,22,23,24,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92  
+3VBSUS 4.24,25,26,38,31,41,42,51,53,62,64,68,81,92  
+3VA 24,31,36,41,43,53,57,64,81,88,93  
+VCCDSW 25,26



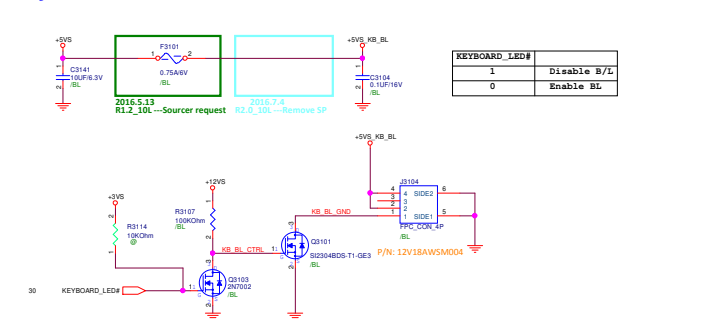
## Fingerprinter



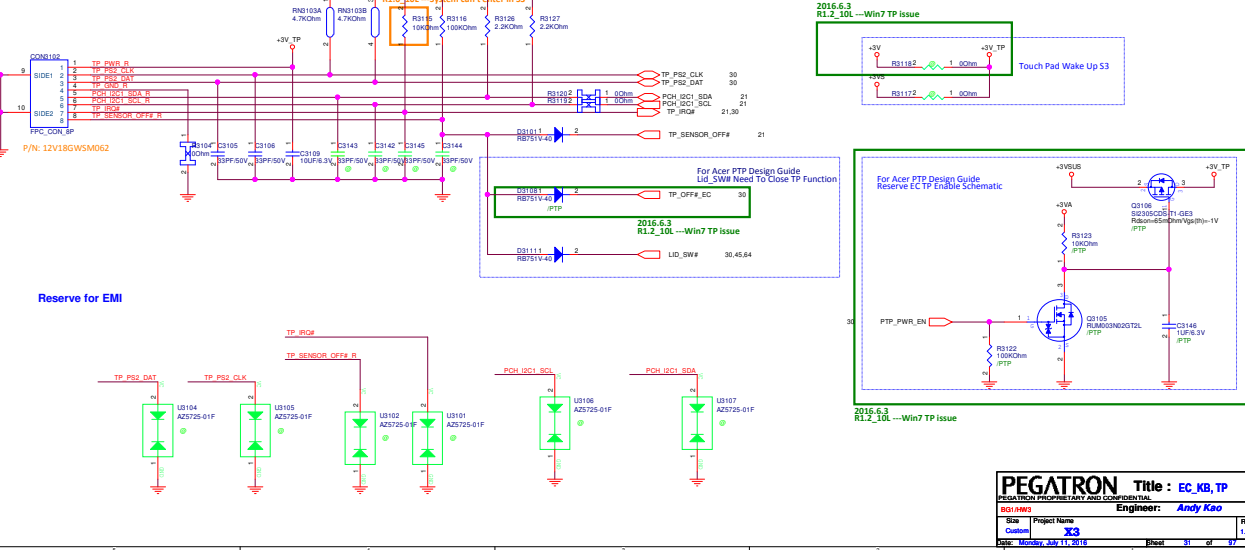
## Keyboard

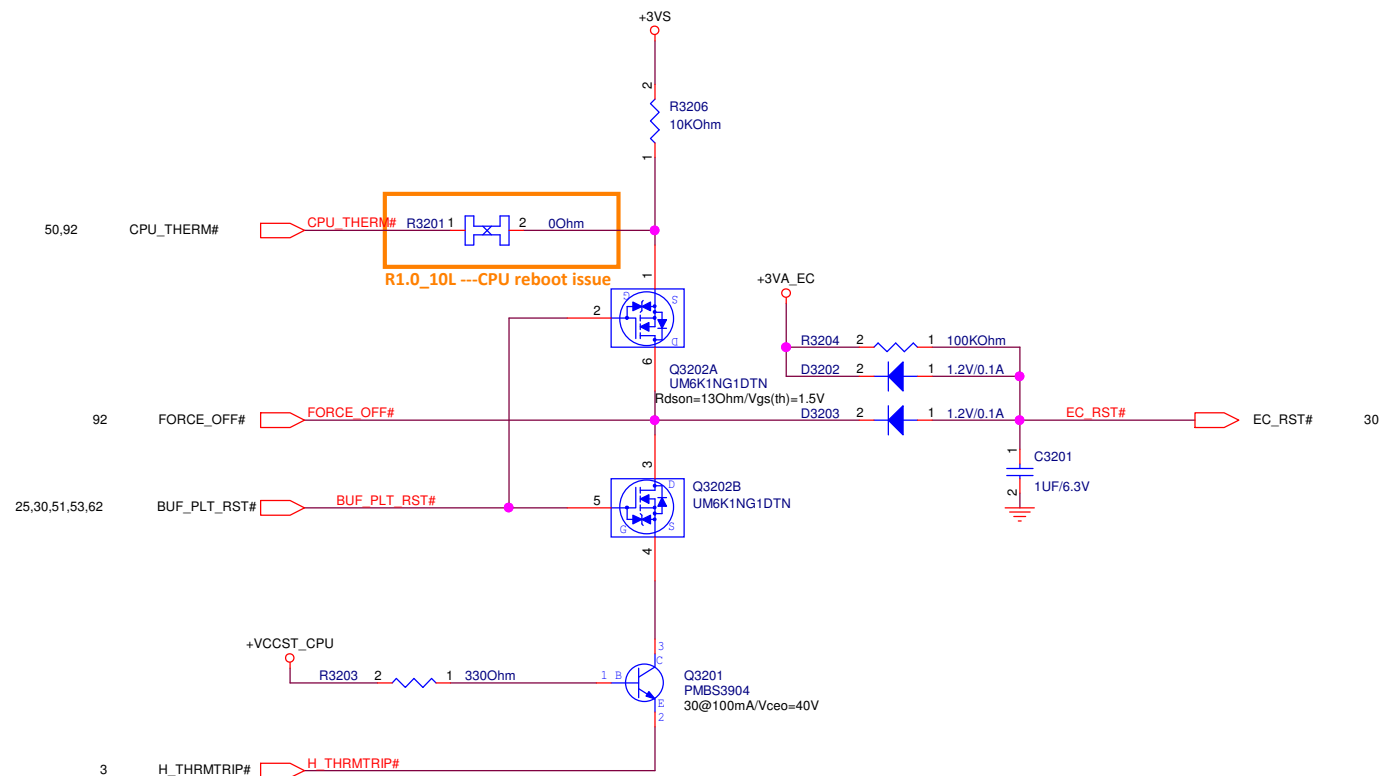


## Keyboard LED



## Click Pad

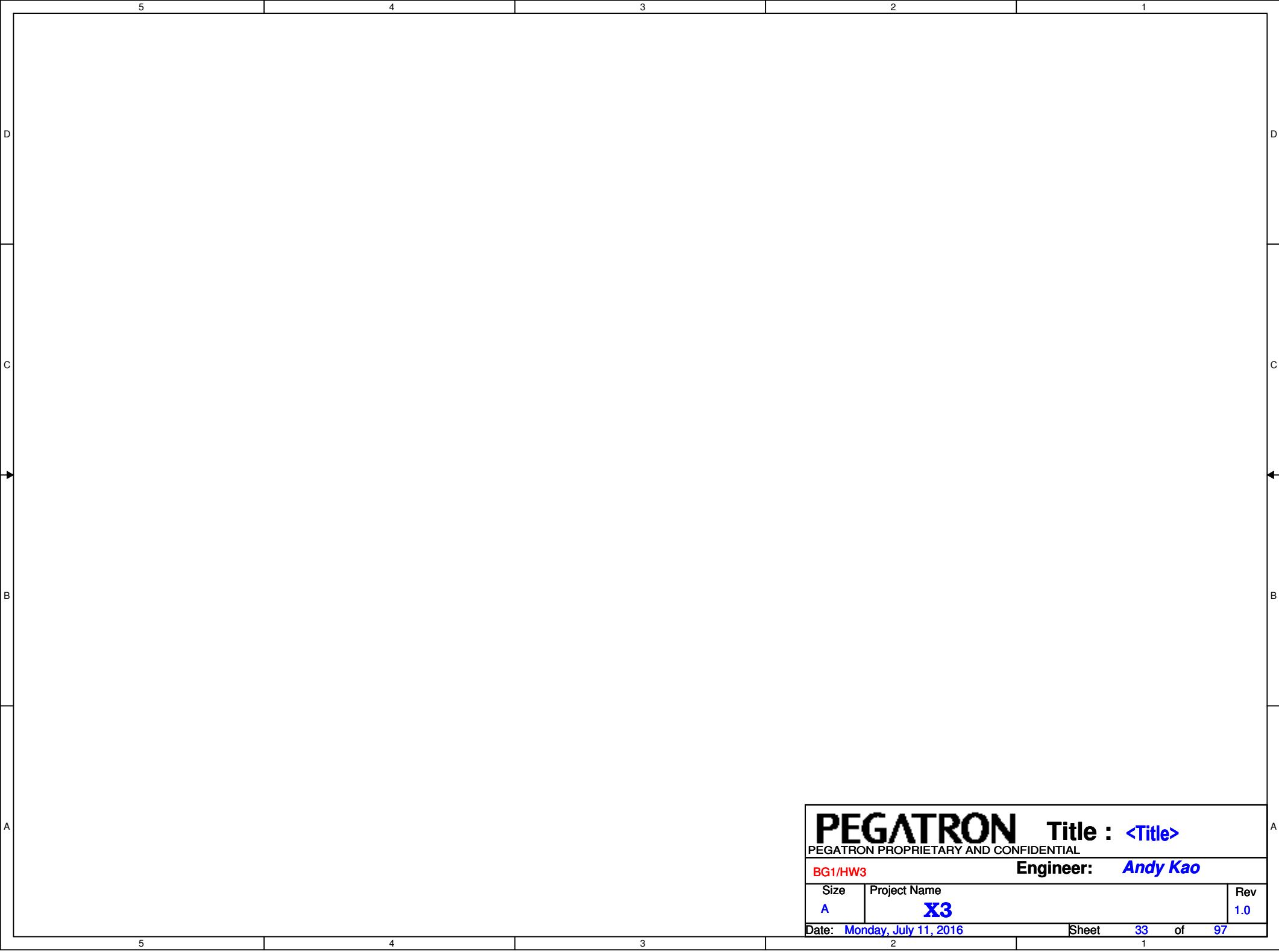




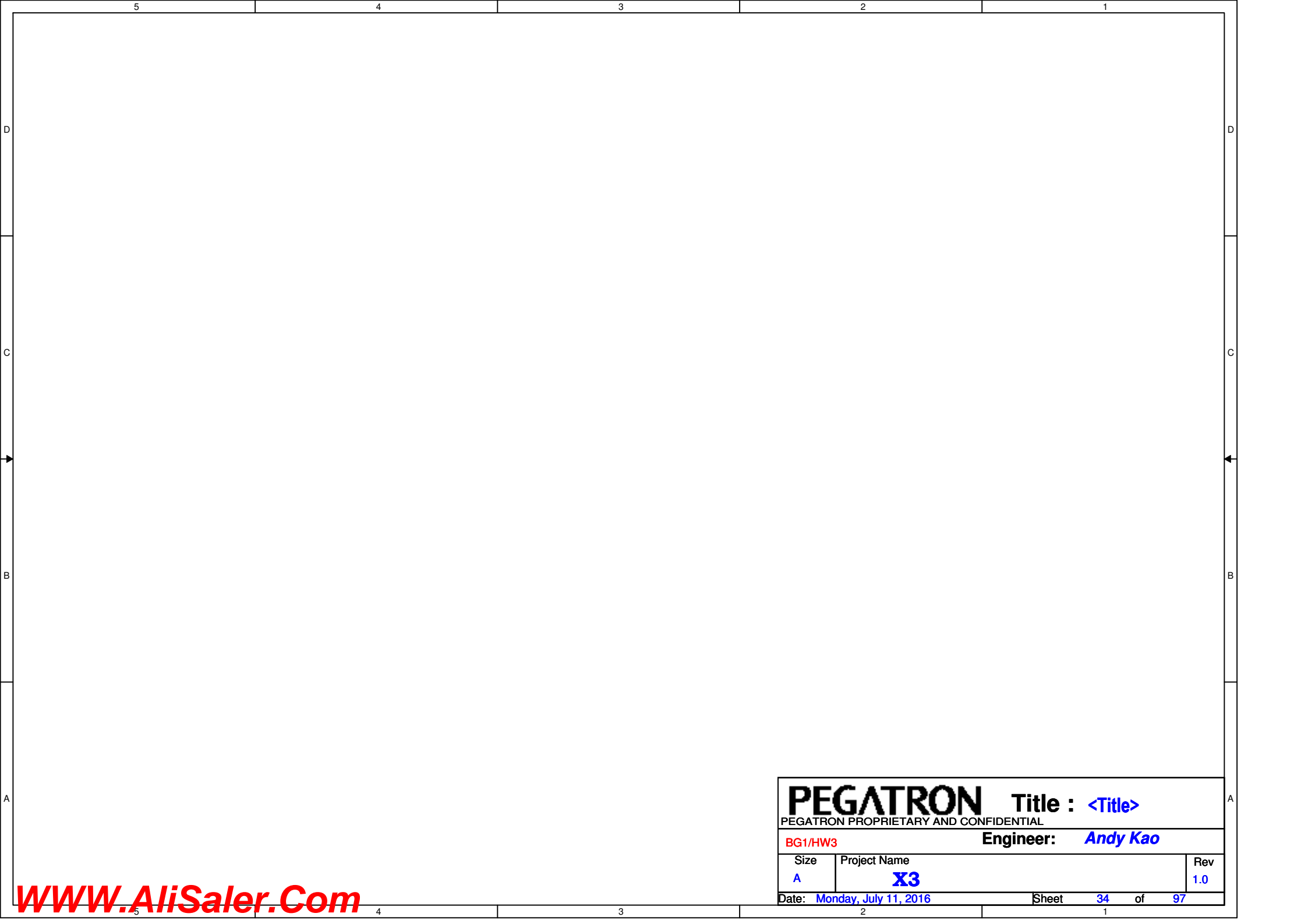
+VCCST\_CPU +VCCST\_CPU 3,5,7,9,25  
+3VA\_EC +3VA\_EC 28,30,44  
+3VS +3VS 3,4,21,22,23,24,30,31,36,37,44,45,47,50,51,53,57,62,64,91,92

<b>PEGATRON</b>		<b>Title :</b> RST_Reset Circuit	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> Andy Kao	
Size B	Project Name <b>X3</b>	Rev 1.0	
Date: Monday, July 11, 2016		Sheet 32 of 97	





<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>33</b> of <b>97</b>



<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	34 of 97

**PEGATRON** Title : <Title>

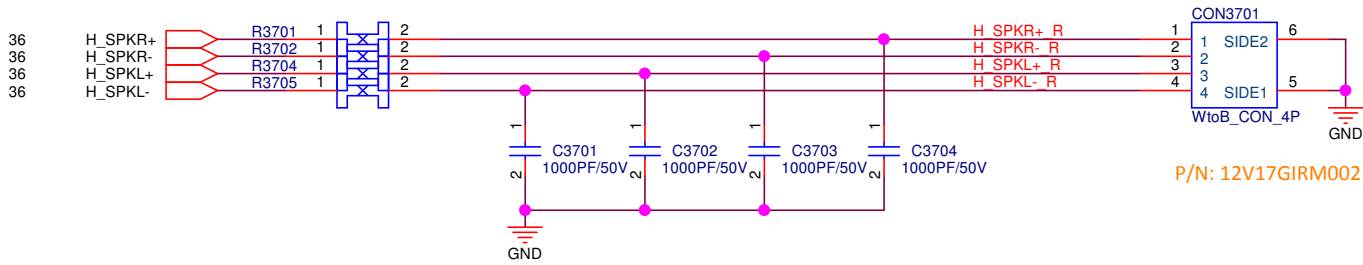
**BG1/HW3**      **Engineer:** *Andy Kao*

Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
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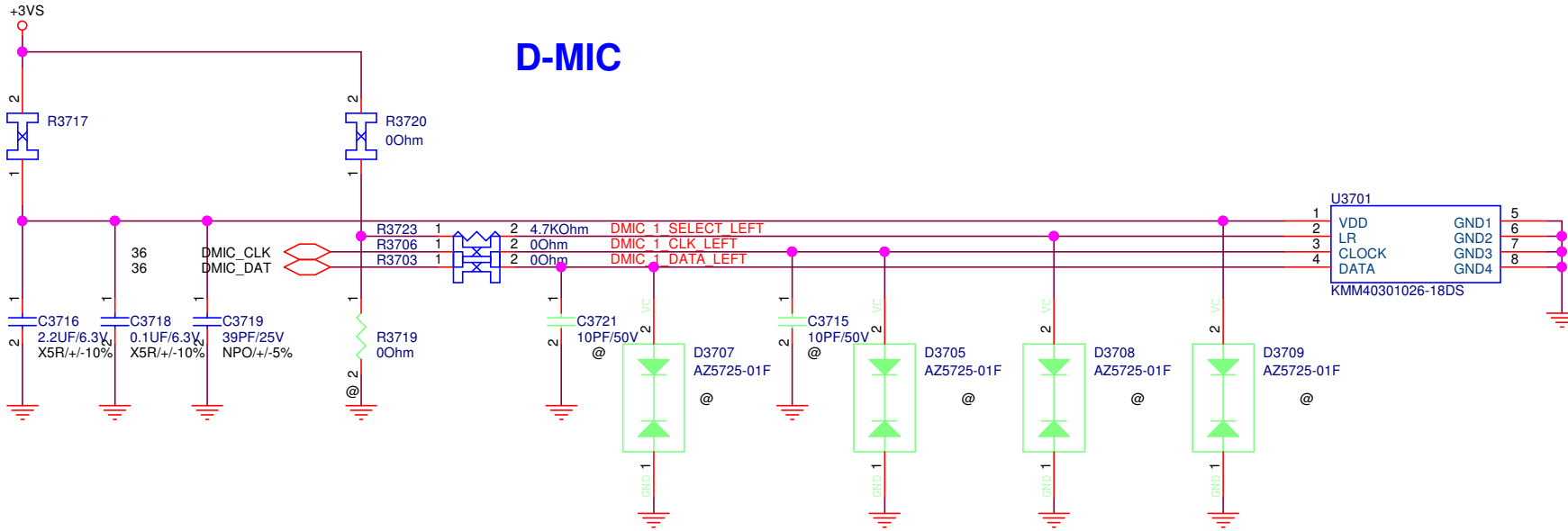
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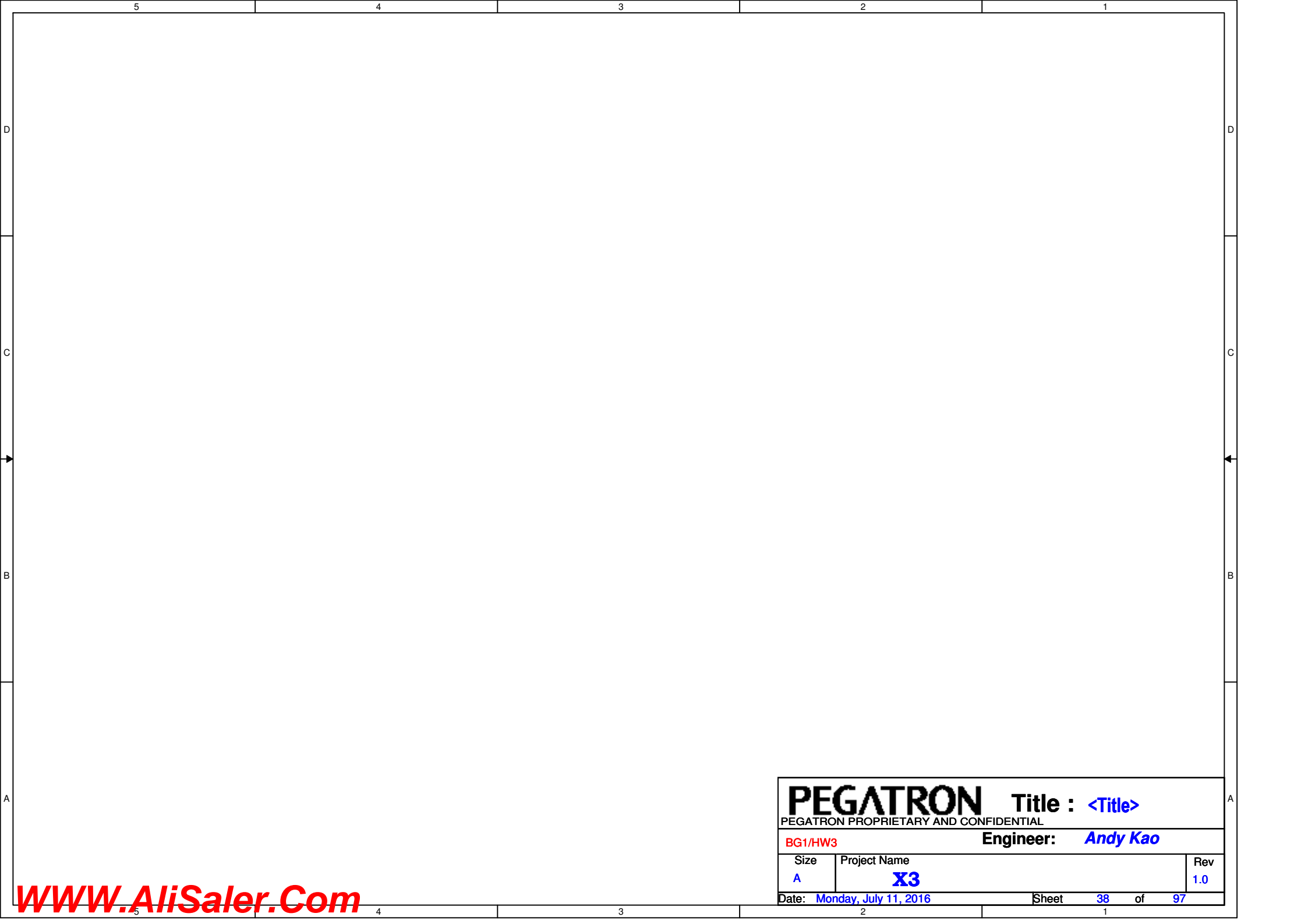


## Speaker

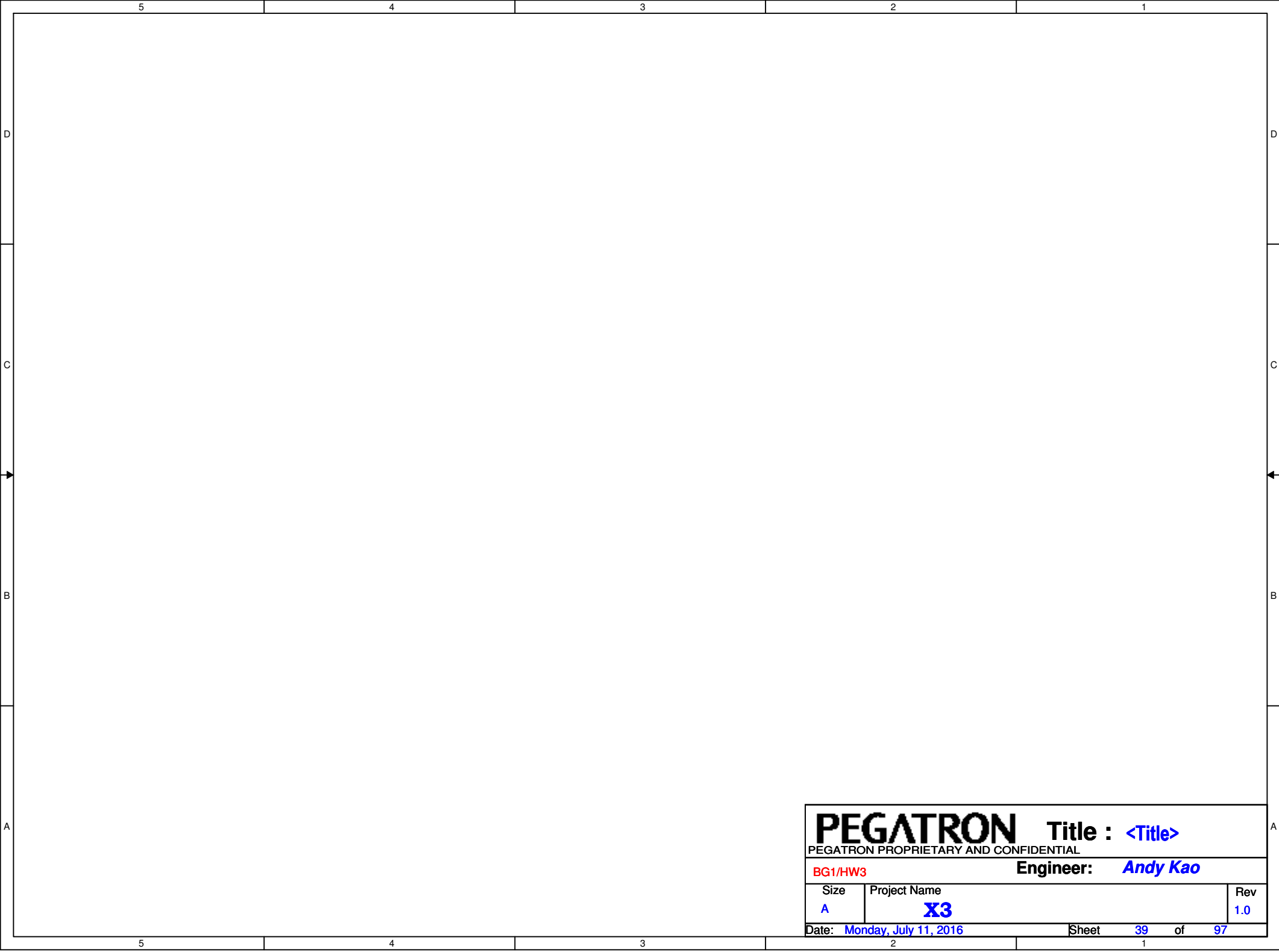


## D-MIC

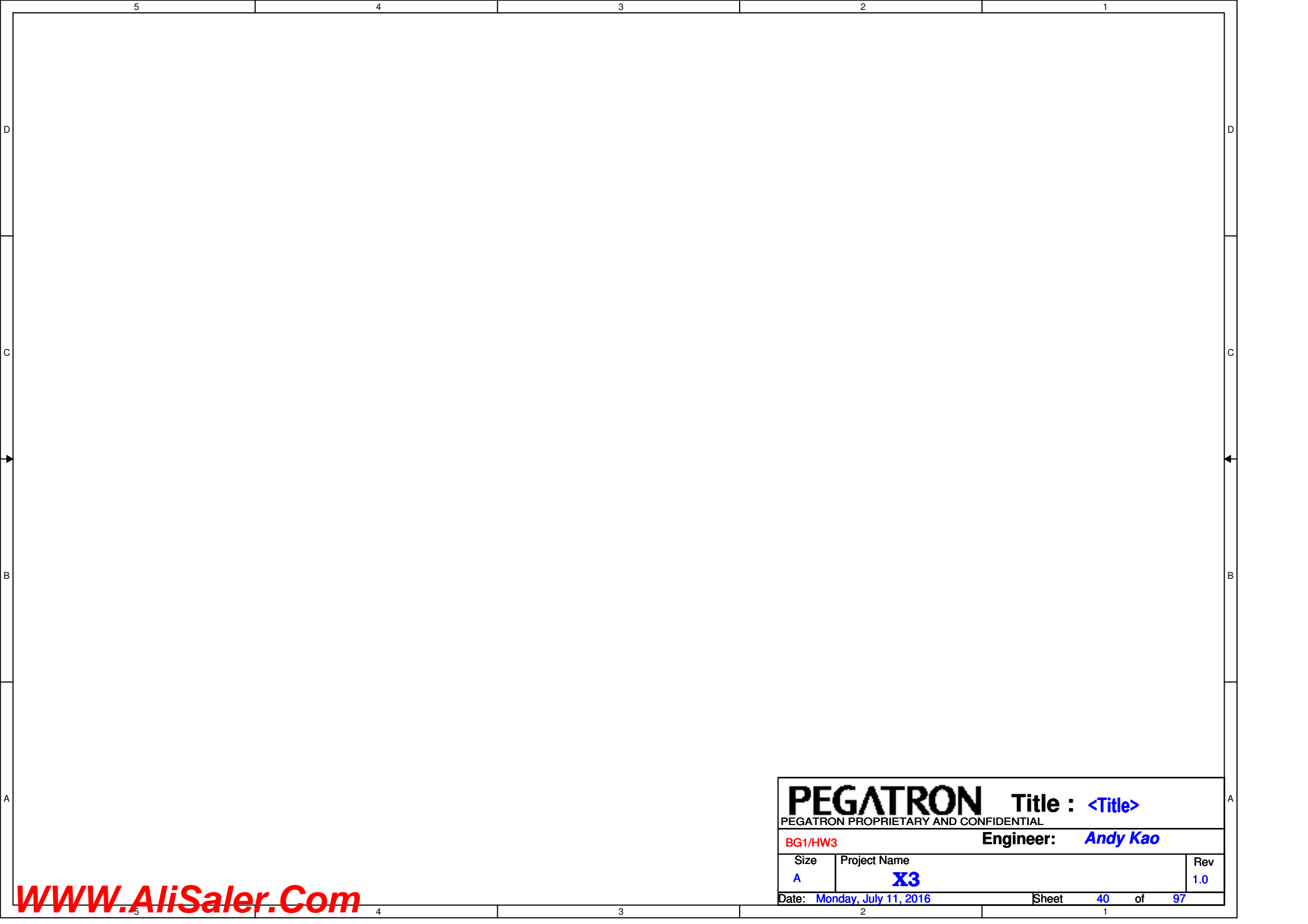




<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	38 of 97

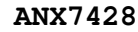
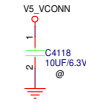


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>39</b> of <b>97</b>



<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>40</i> of <i>97</i>





V5\_VCC0IN is the power source for VCC0IN(UTC\_B5\_CC2 or UTC\_A5\_CC1).

Please make sure:

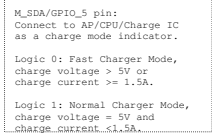
- 1) VCC0IN Voltage range: [4.75V, 5.5V]
- 2) VCC0IN Minimum power is 1W. If DP Alternate Mode is supported, VCC0IN power is up to 1.5W.

Reverse voltage protection is required.

It might be necessary to add a diode to protect the power supply.

Requirement of Q3:

- 1)  $I_d \geq 500\text{mA}$  ( $V_{gs} = -4.5\text{V}$ ).
- 2)  $R_{on} < 120\text{ m}\Omega$  ( $V_{gs} = -4.5\text{V}$ ).
- 3)  $\text{Max } V_{ds} \geq -10\text{V}$



Change to 0650-0084000

CABLE\_DET pin: Connect to AP or CPU.  
Logic 1: USB Type-C cable plug detected.  
Logic 0: USB Type-C cable unplug detected.

INTP\_OUT pin: interrupt output.  
Connect to AP or CPU.

If AP or GPU's interrupt is low triggered, set R16 = 4.7K, leave not installed;  
else if is high level triggered = 4.7K, leave R16 not installed.

R4122  
100KOhm

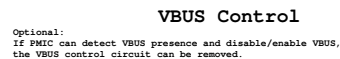
FWR\_EN pin:  
Controlled by AP or CPU  
Logic 1: to power up the chip.  
Logic 0: to power down the chip.

I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

1. The I2C address is determined approximately 500ns after RESET\_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C\_ADR\_0 and I2C\_ADR\_1 pins.
3. If external pull-up resistor is not populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 0.
4. If external pull-up is populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 1.

**PEGATRON** Title: POWER\_FLOWCHART  
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: <b>Andy Kao</b>		
Size <b>C</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		
Sheet <b>41</b> of <b>97</b>		



VBUS\_CTRL Function:

VBUS_CTRL	5V VBUS Output	5=20V VBUS Charge Input
Logic 0	Disable	Enable
Logic 1	Enable	Disable



Note:

1. If battery charger can operate with 5V input, no more circuits are needed.
2. If battery charger needs higher voltage than 5V to operate correctly, ANX74xx should be powered by VBAT and local power.

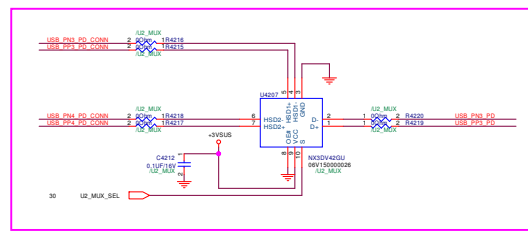
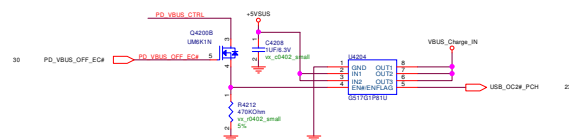
Note:

1. If battery charger can operate with 5V input, no more circuits are needed.
2. If battery charger needs higher voltage than 5V to operate correctly, ANX74xx should be powered by VBAT and local power.

[illegible]

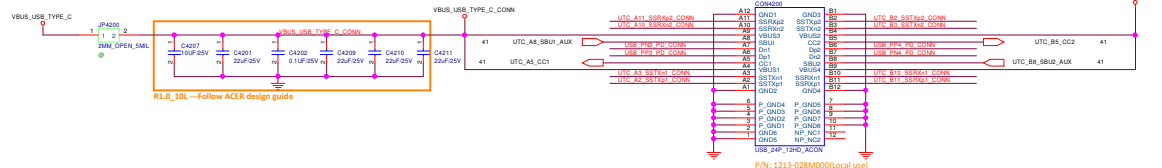
### R1.0\_10L ---Unmount discharge circuit

R1.1\_10L ---PD test fail



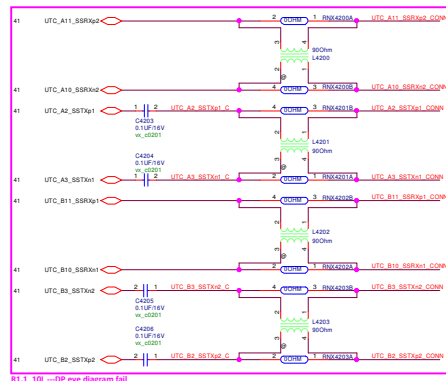
R1.1\_10L ---Reserve for WHO

01.0.10! Fellow ACER design guide

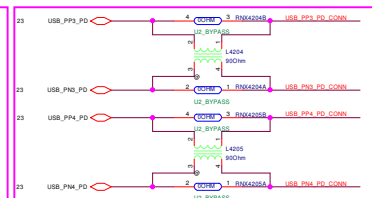


P/N: 1213-028M000(Local use)

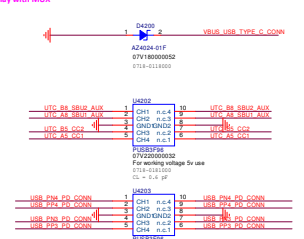
## ESD



81-1 10I —DP eye diagram fail

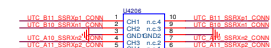
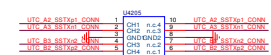


81-1 10I ---Colay with MU







## USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND



## Hardware Solution For Dead Battery

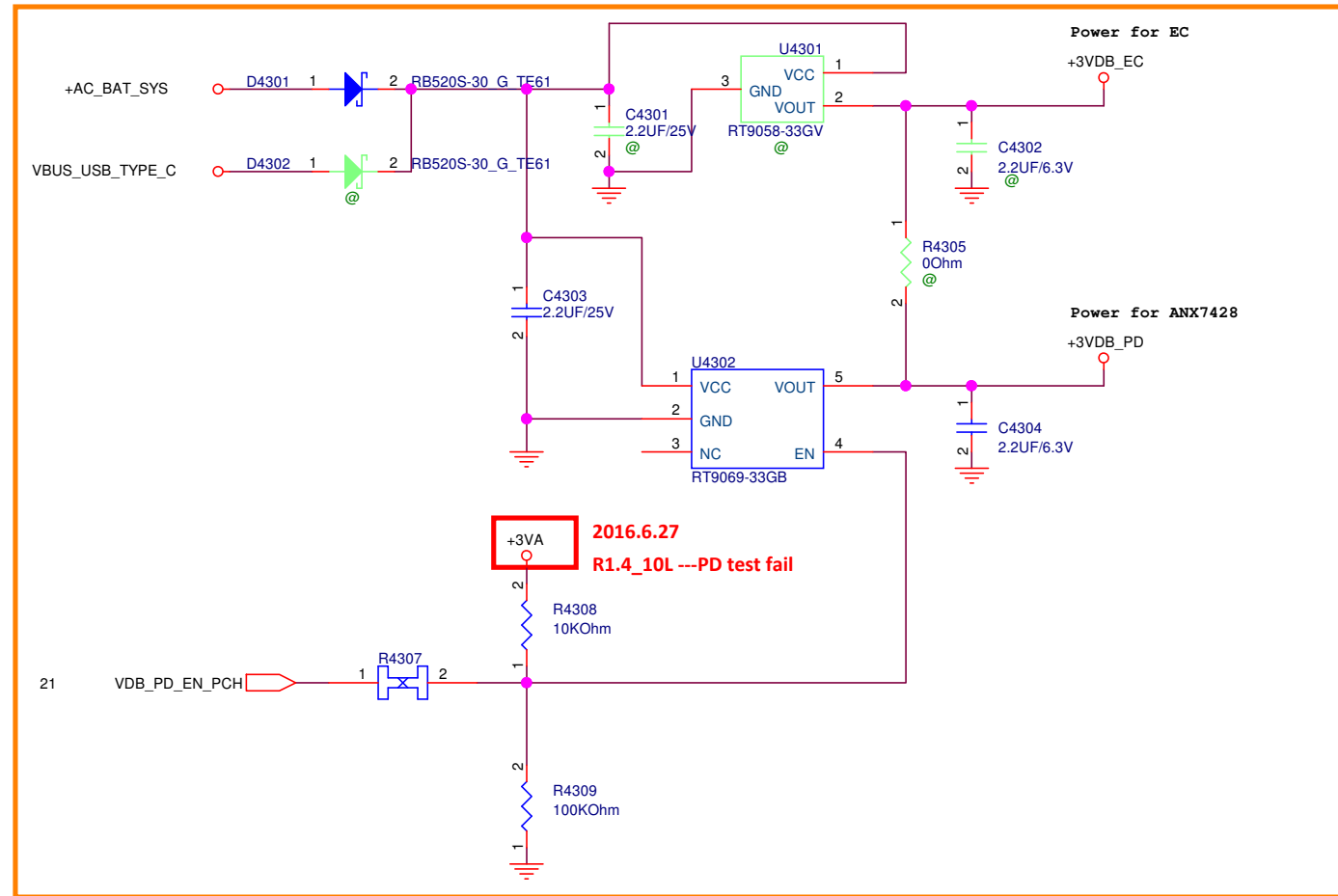
For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	41,42
+AC_BAT_SYS		+AC_BAT_SYS	45,80,81,82,83,88
+3VDB_EC		+3VDB_EC	30
+3VDB_PD		+3VDB_PD	41

Requirement of U1:

- 1) Vin range: 4V-30V.
- 2) Vout: EC's operating voltage + Vf of D1
- 3) Output current  $\geq$  EC's operating current.

**R1.0\_10L ---Follow HAWAll type-c design**



<Variant Name>

# PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

**Title :** Dead Battery

**Engineer:** **Andy Kao**

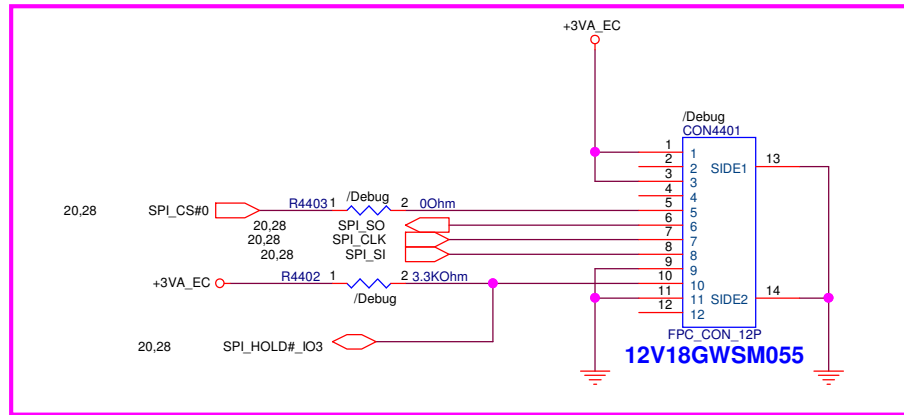
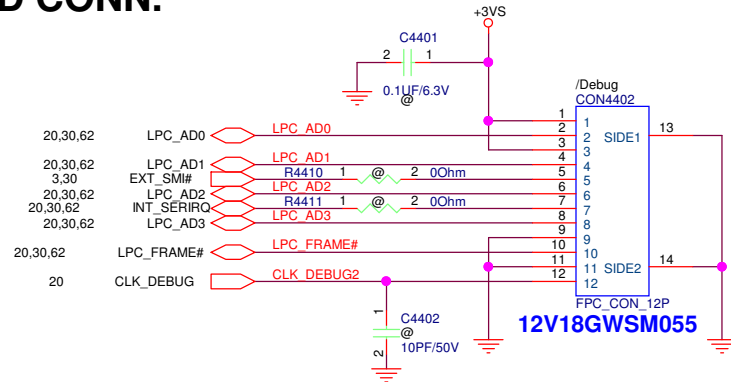
Size Custom	Project Name
----------------	--------------

### X3

Rev  
1.0

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# DEBUG CARD CONN.

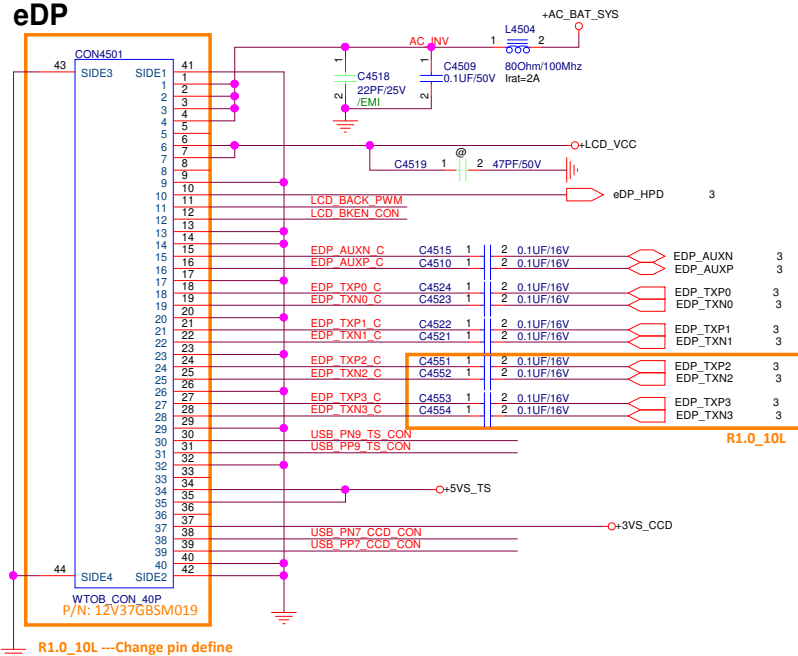


R1.1\_10L ---BIOS request

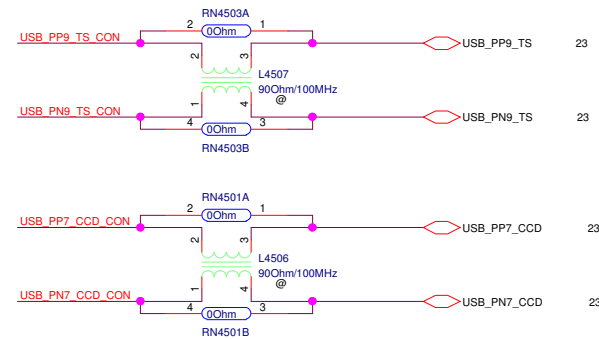
<Variant Name>

<b>PEGATRON</b>		<b>Title :</b> <b>DEBUG CONN.</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size	Project Name		Rev
<b>B</b>	<b>X3</b>		<b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>44</b> of <b>97</b>	

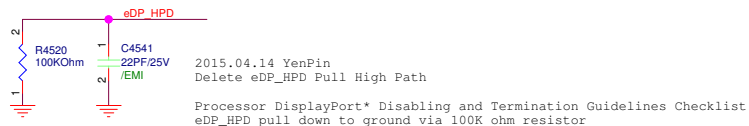
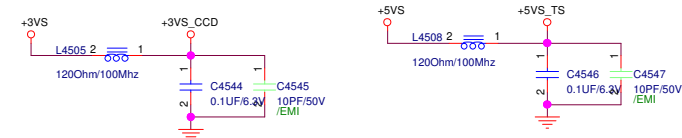
# eDP



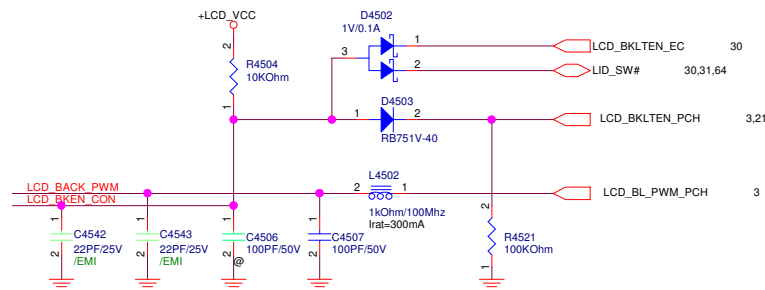
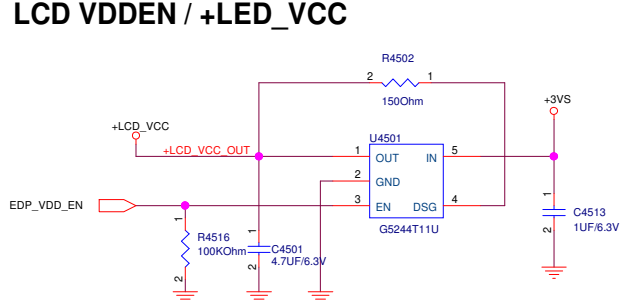
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,48,50,51,57,80,91
+AC_BAT_SYS	+AC_BAT_SYS	43,80,81,82,83,88



## Camera

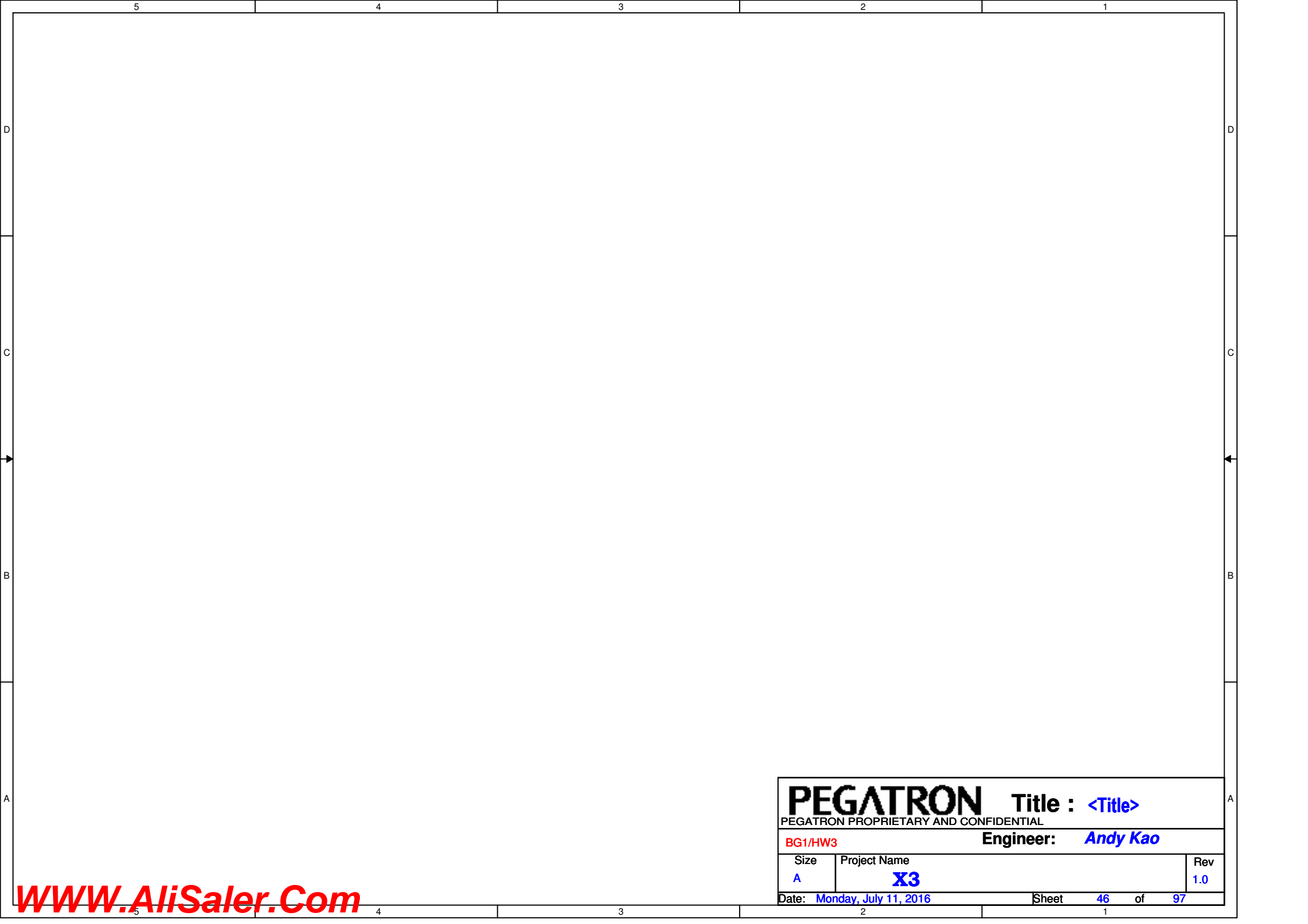


## LCD VDDEN / +LED\_VCC



<Variant Name>

<b>PEGATRON</b>		Title : <b>eDP CONN</b>	
Size	Project Name	Engineer:	<b>Andy Kao</b>
Custom	<b>X3</b>		
Date: Monday, July 11, 2016	Sheet	45	of 97
	Rev	1.0	



<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	46 of 97

T4702 1 PRE

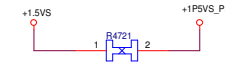
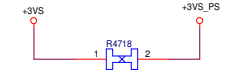
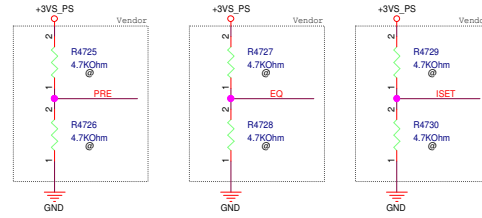
Output pre-emphasis setting; Internal pull down at -150kΩ, 3.3V I/O.  
L: no pre-emphasis  
H: 1.6dB pre-emphasis  
M: 2.5dB pre-emphasis

T4701 1 EQ

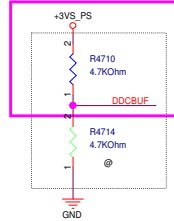
Receiver equalization setting; Internal pull down at -150kΩ, 3.3V I/O.  
L: programmable EQ for channel loss up to 12.6dB  
H: programmable EQ for channel loss up to 4.3dB  
M: programmable EQ for channel loss up to 8.6dB

T4703 1 ISET

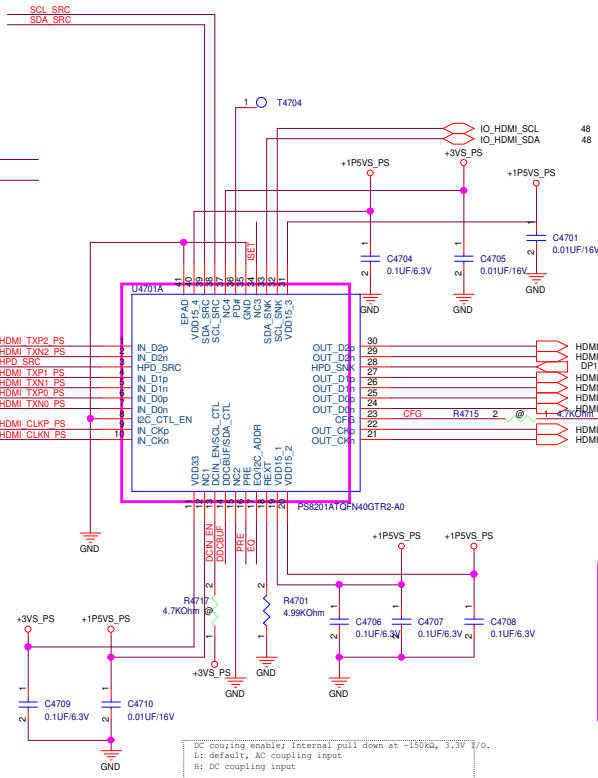
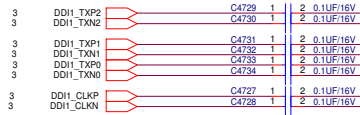
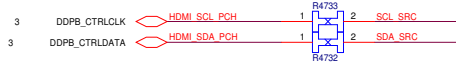
TMDS output swing adjustment; Internal pull down at -150k, 3.3V I/O.  
L: default  
H: increase +13%  
M: reduce -13%



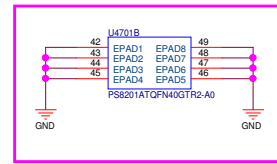
R1.1\_10L ---Follow megatron



Enable active DDC buffer; Internal pull down at -150kΩ, 3.3V I/O.  
L: default, passive DDC pass-through  
H: active DDC buffer with default threshold  
M: active DDC buffer without internal pull up resistor



Configuration pin, 3.3V I/O, internal pull down at -150k, 3.3V I/O.  
L: HDMI ID disable  
H: HDMI ID enable  
(Typ:1.5V; Max:1.53V; Min:1.47V)

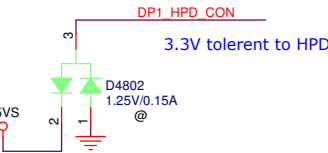
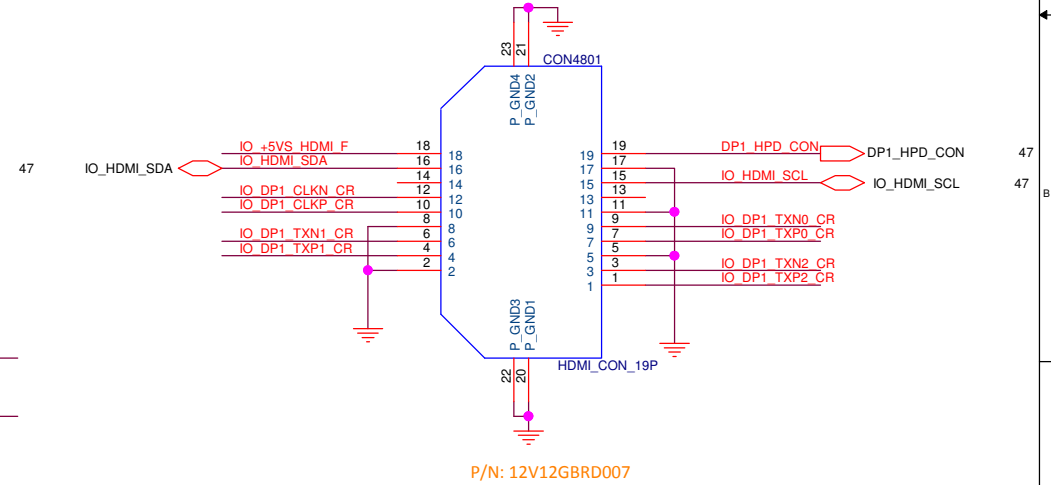
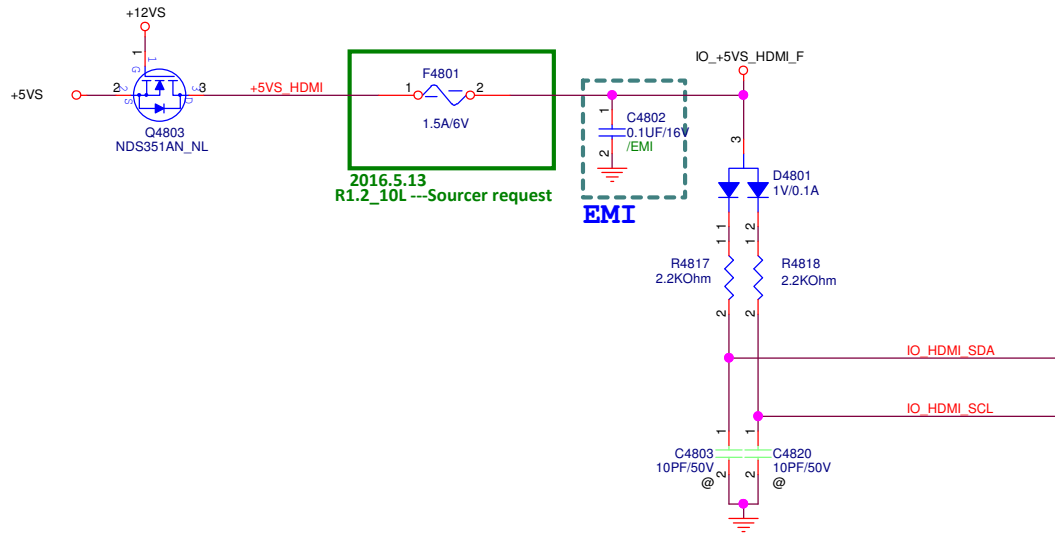


R1.1\_10L ---Sourcer request

DC coupling enable; Internal pull down at -150kΩ, 3.3V I/O.  
L: default, AC coupling input  
H: DC coupling input

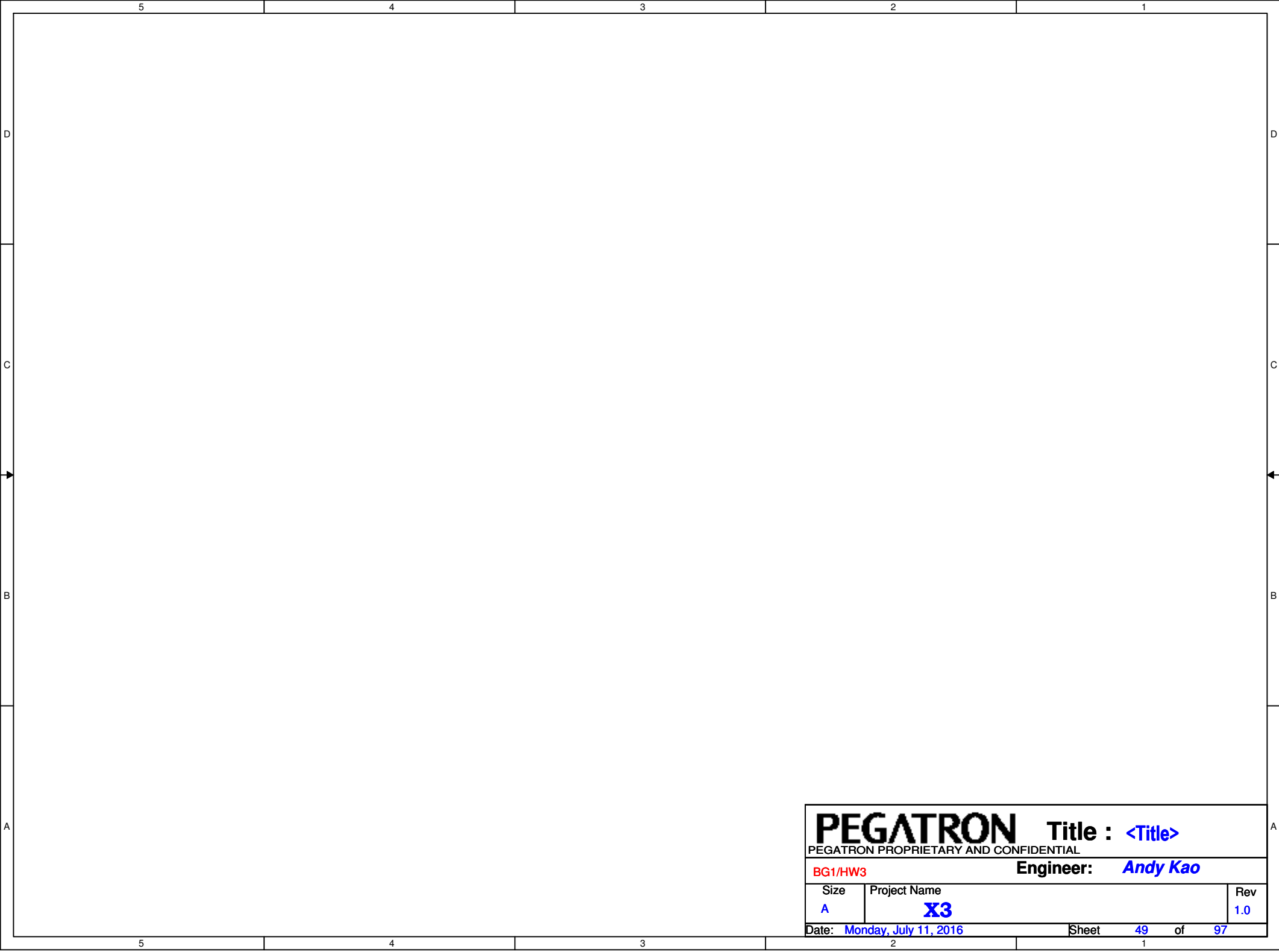
# HDMI

+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+5VS	31,36,45,50,51,57,80,91
+12VS	31,57,91



<b>PEGATRON</b>		Title : <b>HDMI-4K2K</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Andy Kao</b>	
Size B	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>48</b>	of <b>97</b>



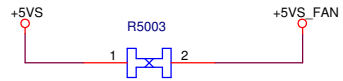
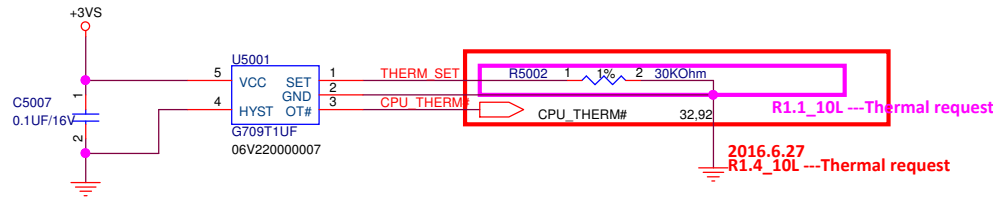


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>49</b> of <b>97</b>

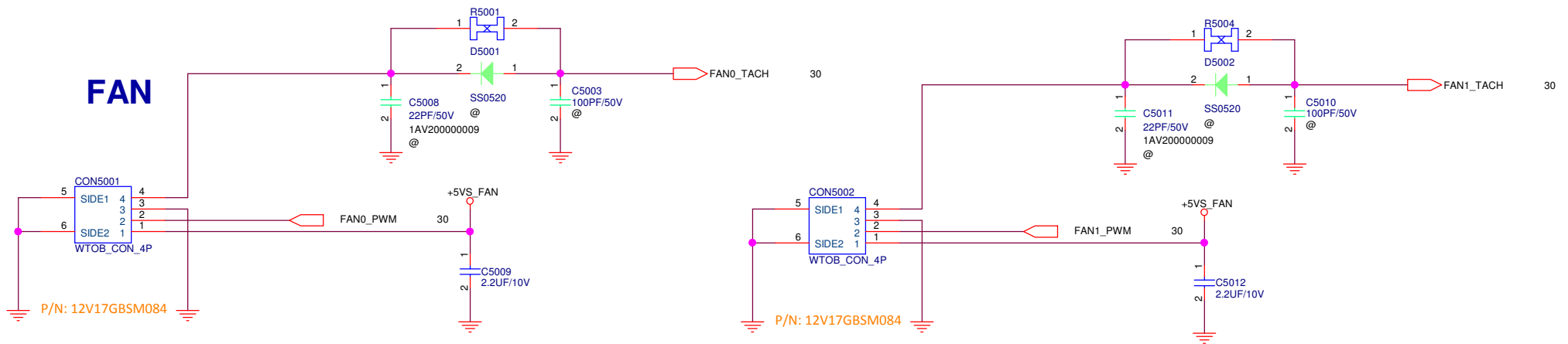
# Thermal Sensor

temp setting : 80 degree

$RSET(k\Omega) = 0.0012T^{\circ}C - 0.9308T + 96.147$



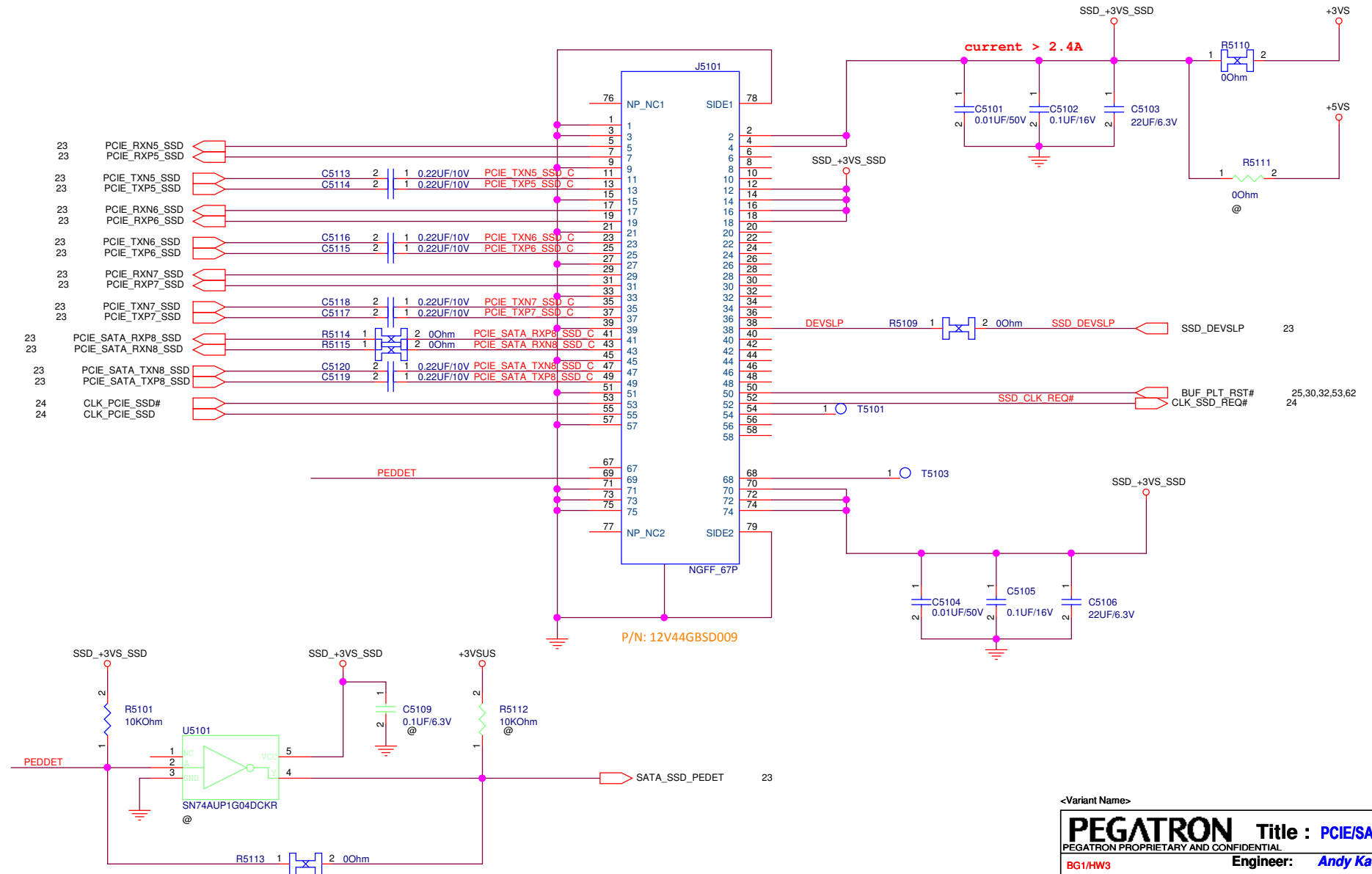
## FAN



<Variant Name>

<b>PEGATRON</b>		Title : Thermal/Fan	
BG1/HW3		Engineer: Andy Kao	
Size	Project Name	Rev	
B	X3	1.0	
Date: Monday, July 11, 2016		Sheet	50 of 97

## SSD(SATA/PCIE x4) NGFF socket (M-key)



**<Variant Name>**

**PEGATRON** Title : **PCIe/SATA SSD**

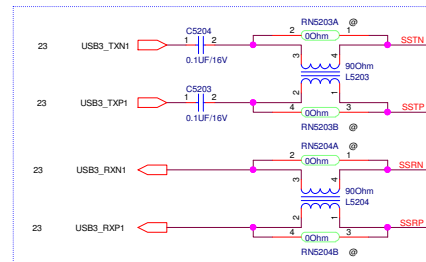
**Engineer:** *Andy Kao*

Size	Project Name	Rev
Custom	<b>X3</b>	1.0

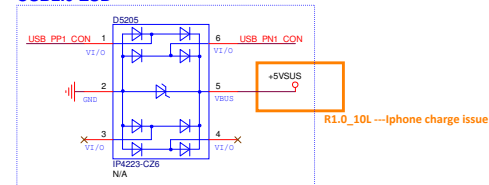
Date: Monday, July 11, 2016 Sheet 51 of 97

## USB 3.0

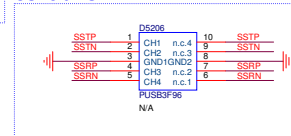
### USB3.0 Choke



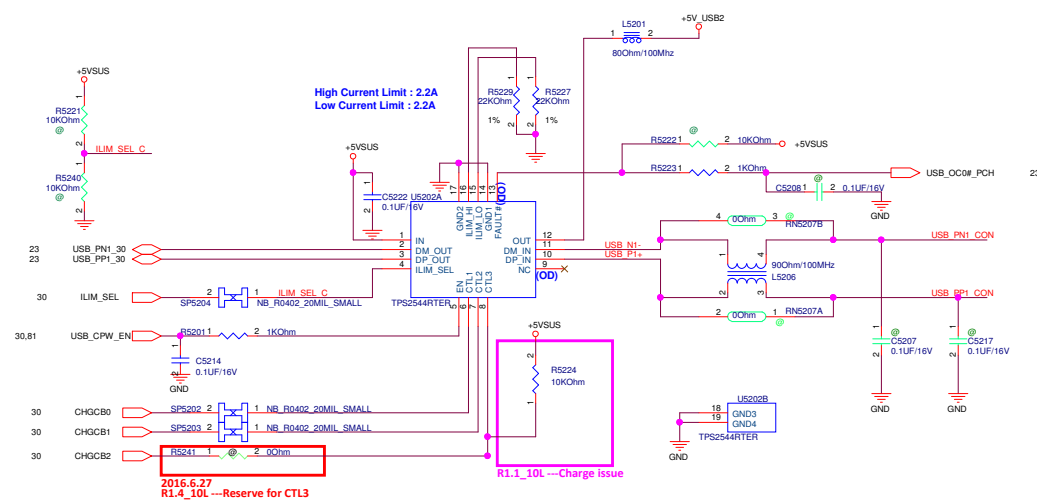
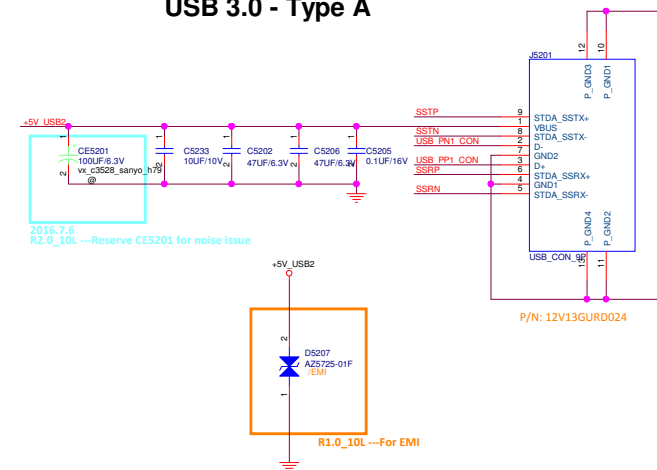
## USB2.0 ESD



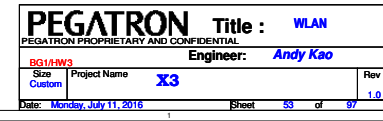
## USB3.0 ESD



## USB 3.0 - Type A

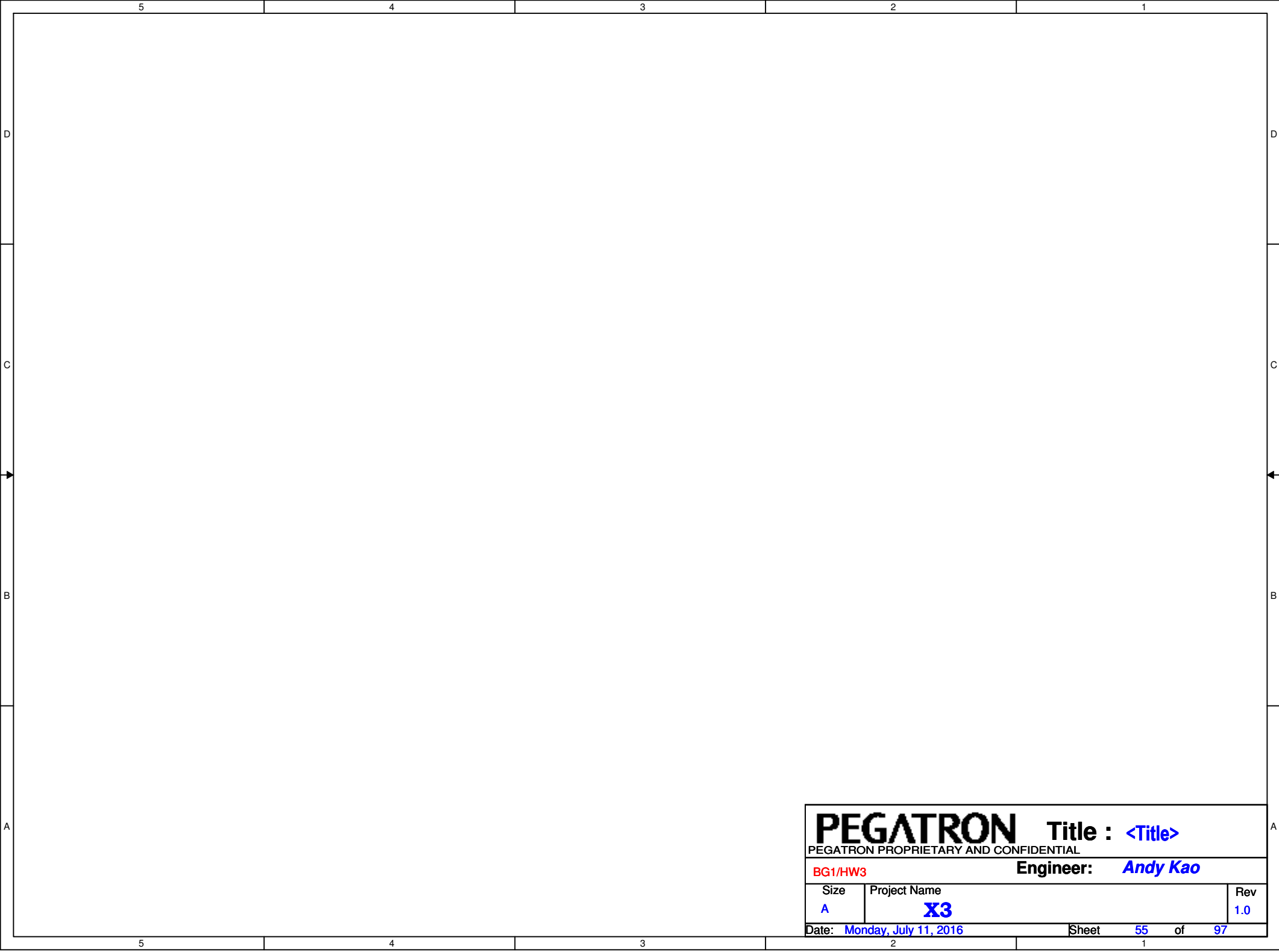


+3VS  +3VS 3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,57,62,64,91,92



	5	4	3	2	1
D					D
C					C
B					B
A					A

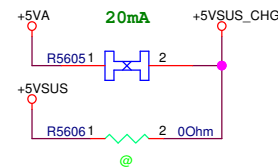
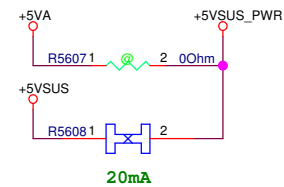
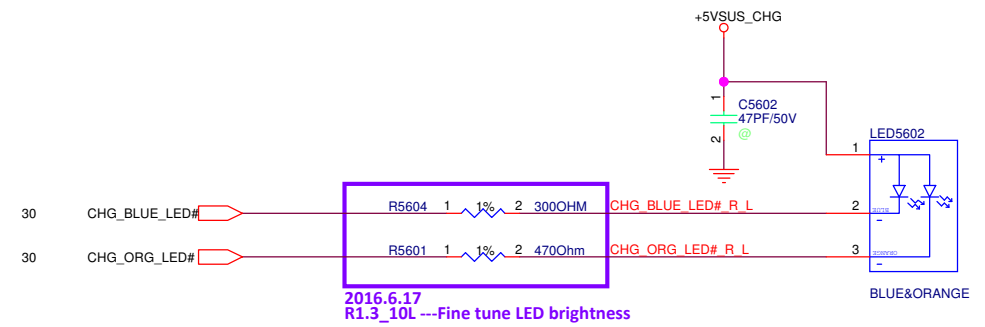
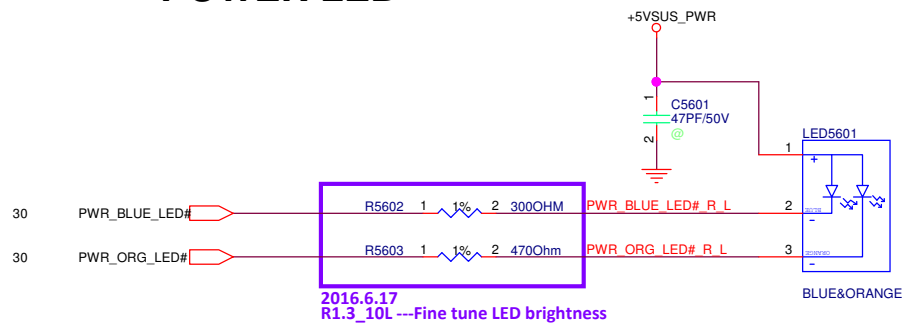
<div> <div>PEGATRON</div> <div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div> </div>		<div> <div>Title :</div> <div>USB HUB</div> </div>	
<div> <div>&lt;OrgName&gt;</div> </div>		<div> <div>Engineer:</div> <div>Andy Kao</div> </div>	
<div> <div>Size</div> <div>A</div> </div>	<div> <div>Project Name</div> <div>X3</div> </div>		<div> <div>Rev</div> <div>1.0</div> </div>
<div> <div>Date:</div> <div>Monday, July 11, 2016</div> </div>		<div> <div>Sheet</div> <div>54</div> <div>of</div> <div>97</div> </div>	



<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <b>X3</b>		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>55</i> of <i>97</i>	

## POWER LED

## Charger LED

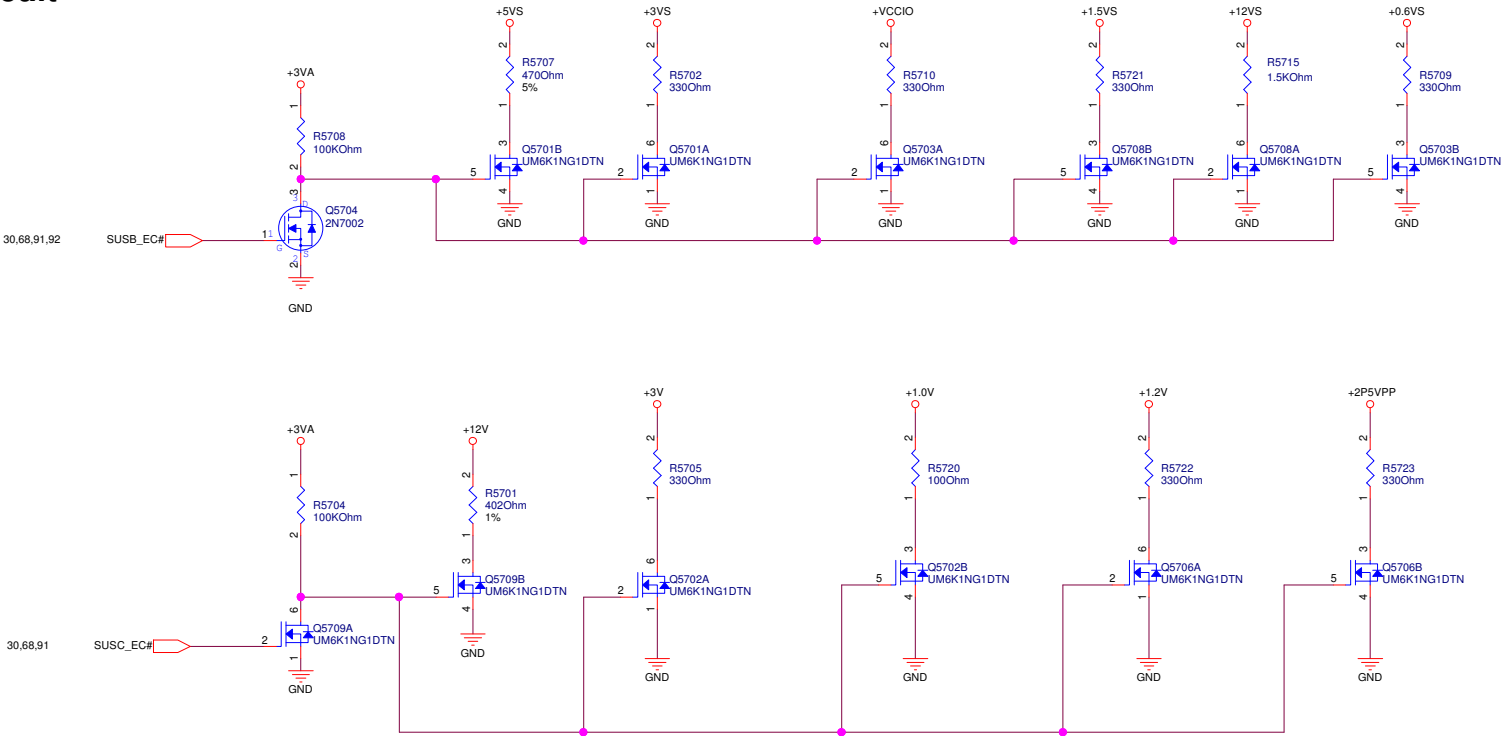


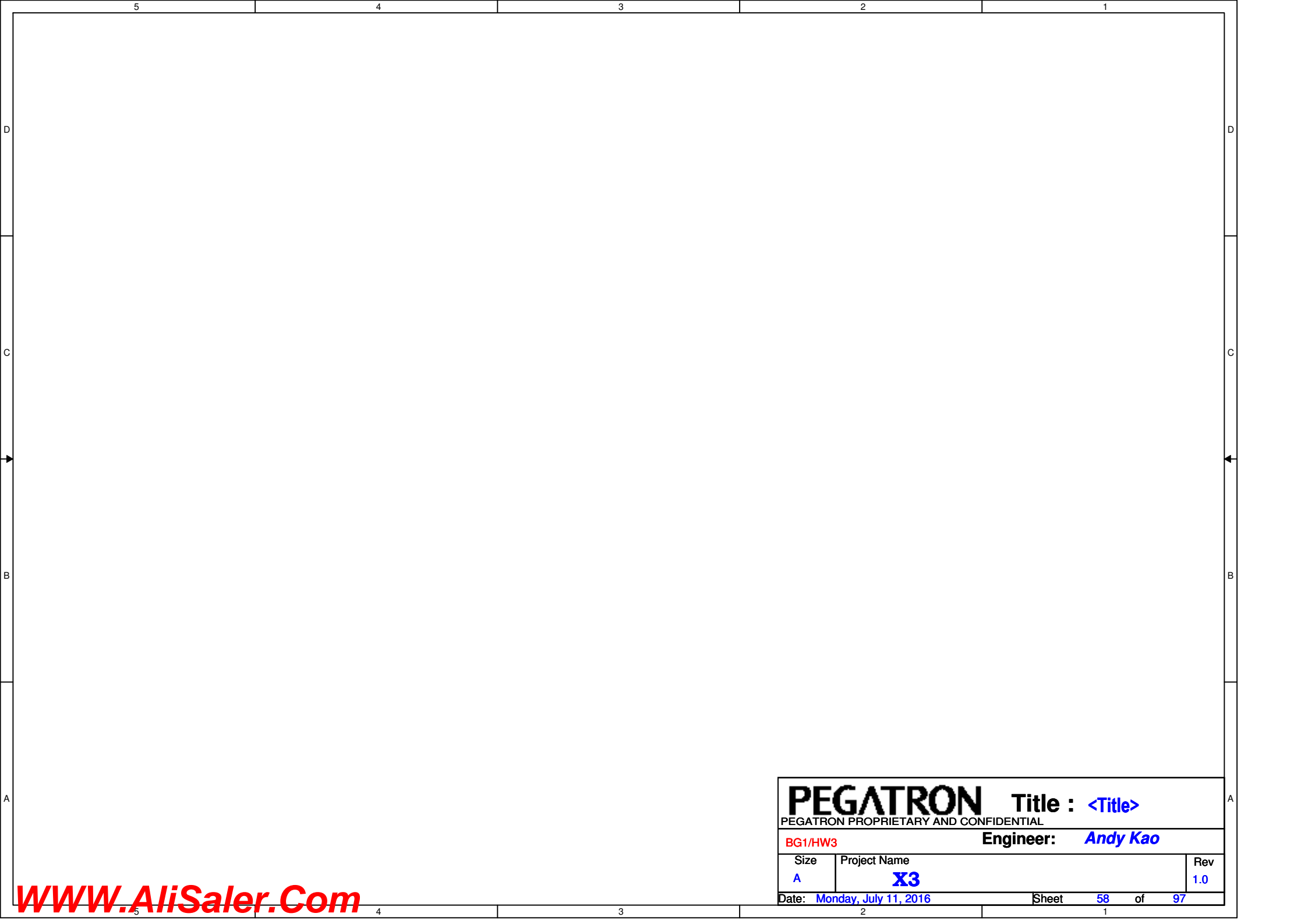
<Variant Name>

<b>PEGATRON</b>		<b>Title : LED_Indicator</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer: Andy Kao</b>	
Size <b>B</b>	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>56</b> of <b>97</b>	

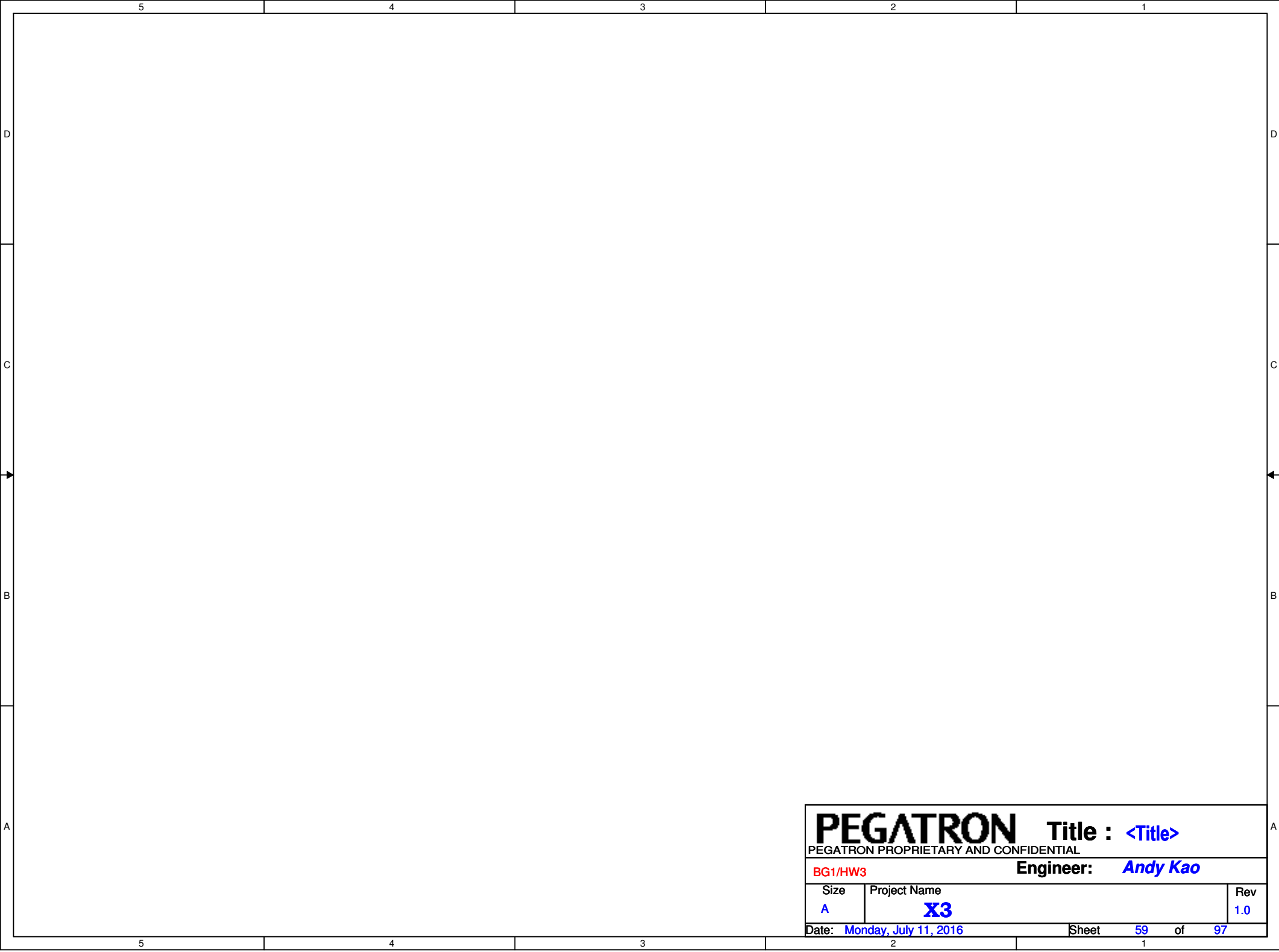


Discharge Circuit



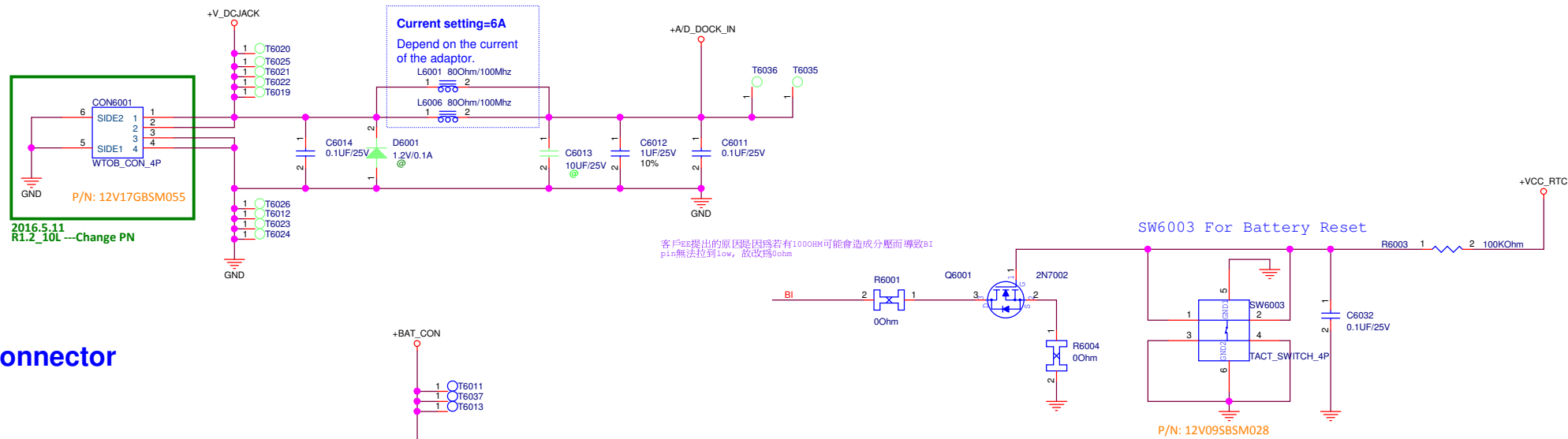


<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	58 of 97

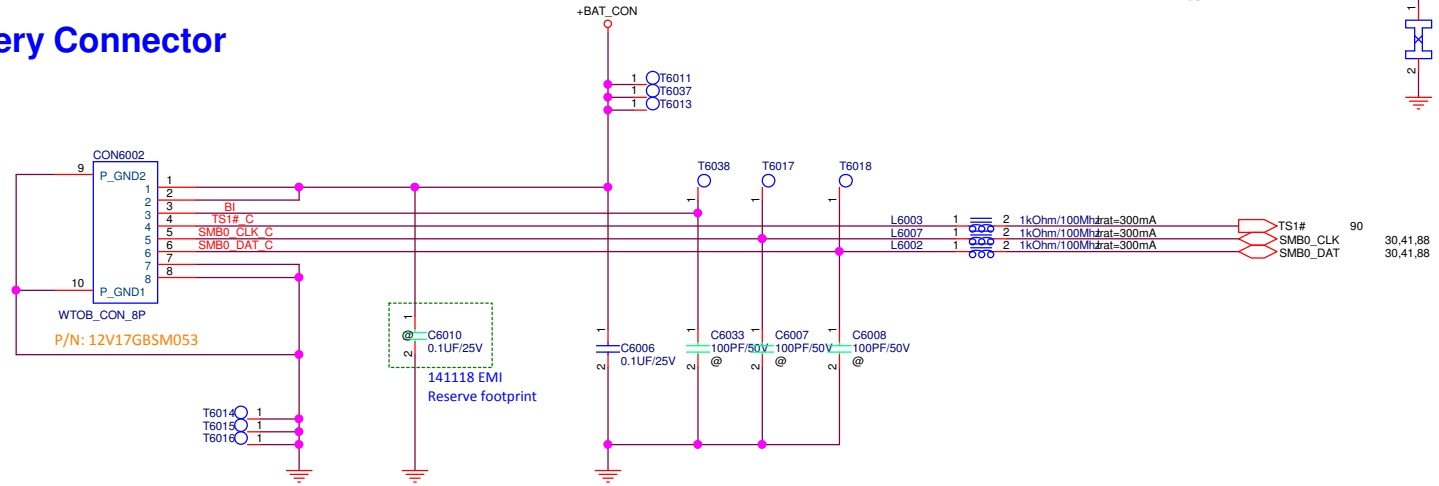


<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <b>X3</b>		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>59</i> of <i>97</i>	

DC Jack WtoB CONN

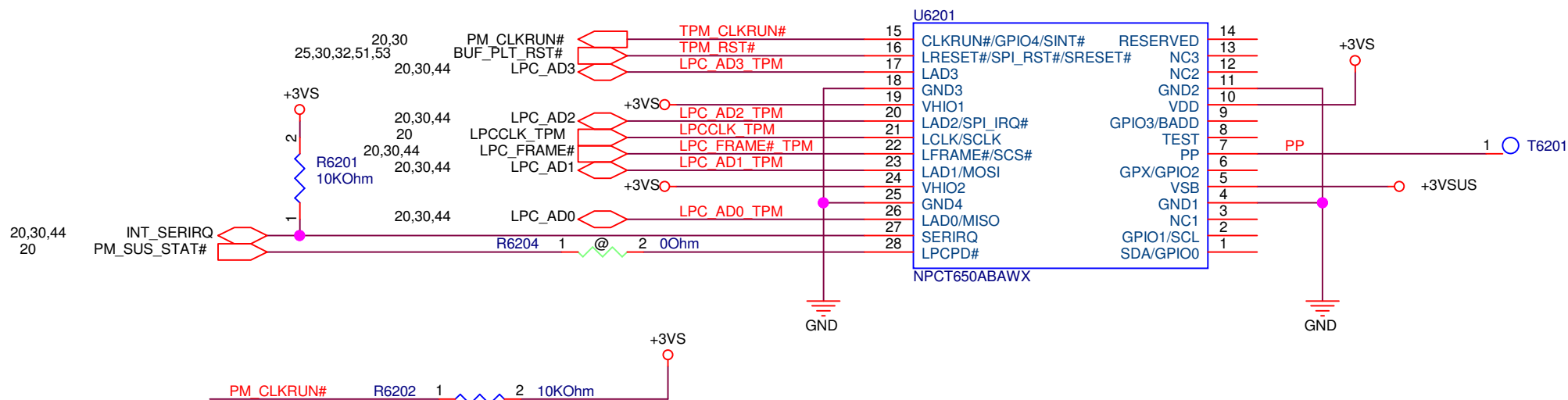
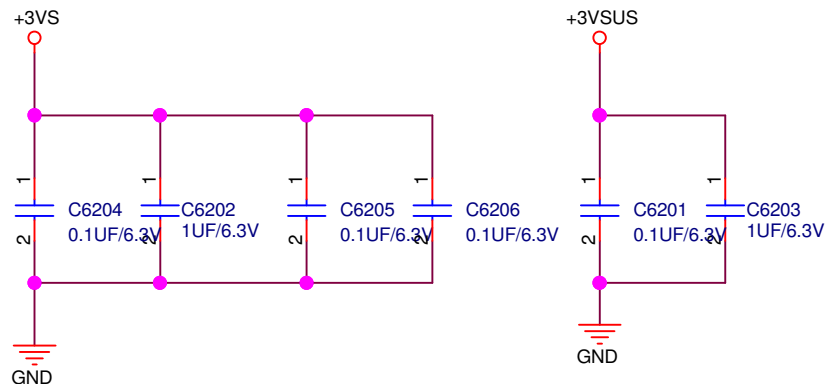


Battery Connector



PEGATRON				Title : DC_IN/BAT CONN	
BG1/HW3		Engineer: Andy Kao			
Size	Project Name			Rev	
Custom	X3			1.0	
Date: Monday, July 11, 2016		Sheet 60 of 97			

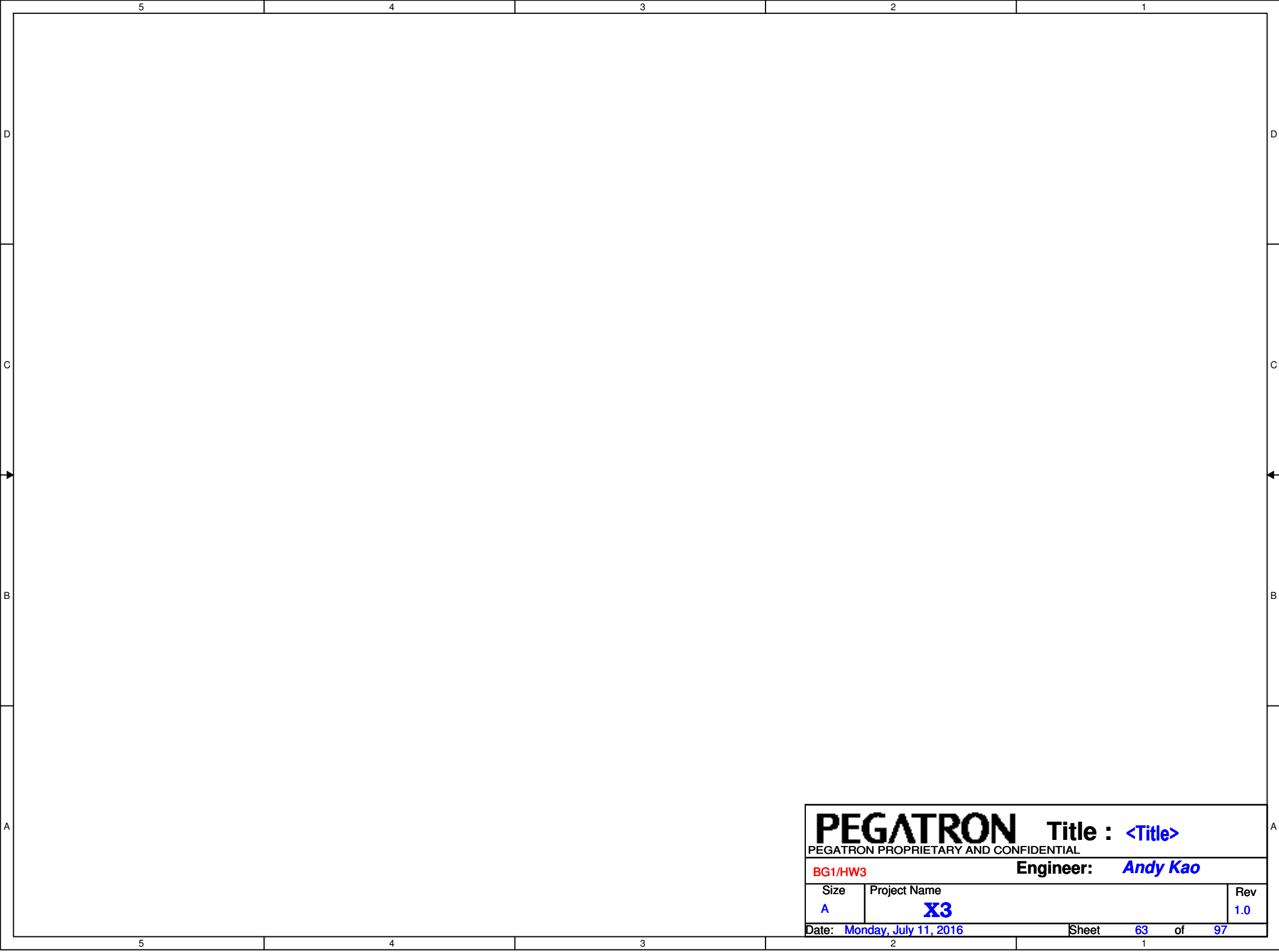
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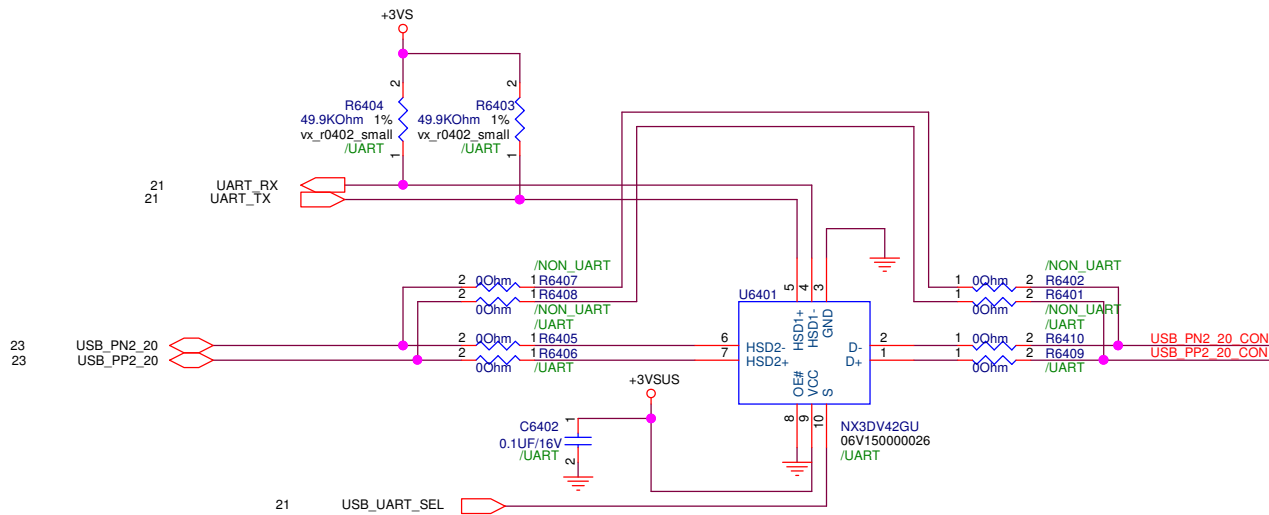
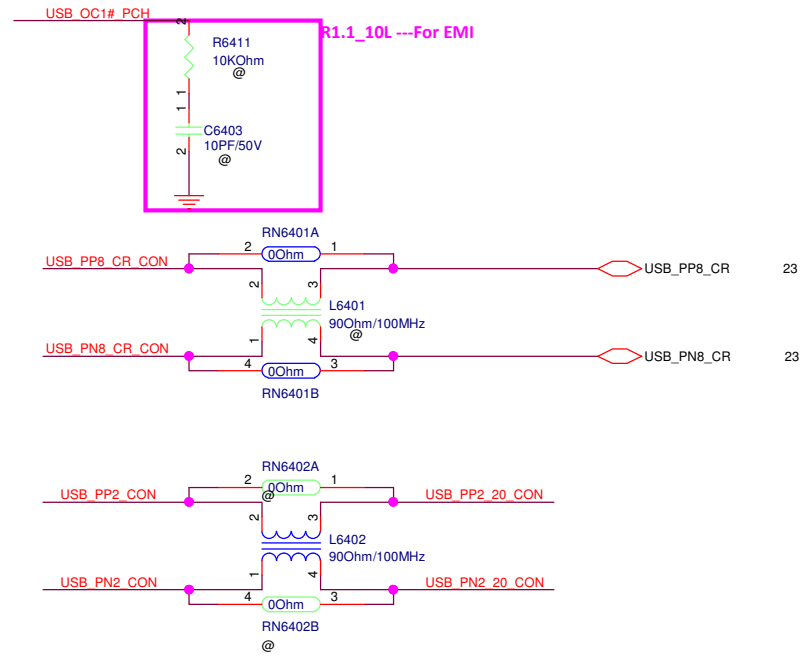
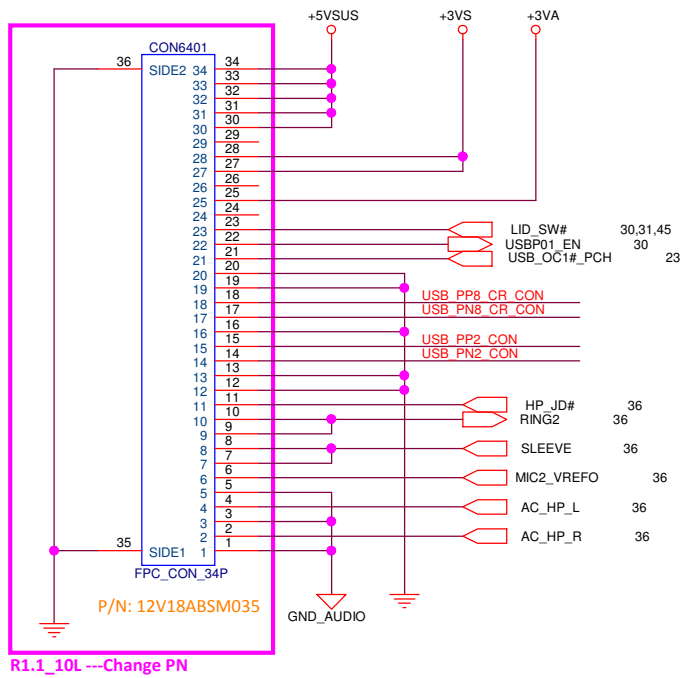
Vendor Suggest Pull High Resistor Need To Close To TPM  
PM\_CLKRUN#, INT\_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

<b>PEGATRON</b>		Title : <b>TPM CONN</b>	
BG1/HW3		Engineer: <b>Andy Kao</b>	
Size Custom	Project Name <b>X3</b>		Rev 1.0
Date: <b>Monday, July 11, 2016</b>		Sheet <b>62</b> of <b>97</b>	



<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <b>X3</b>		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>63</i> of <i>97</i>	



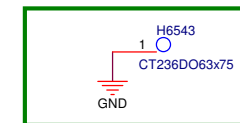
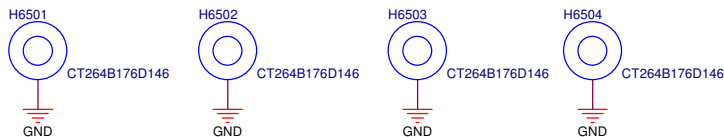
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<b>PEGATRON</b>		Title : <b>IO CON.</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Andy Kao</b>	
Size <b>B</b>	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>64</b> of <b>97</b>	



# CPU NUT

6\*2.5mm\*1

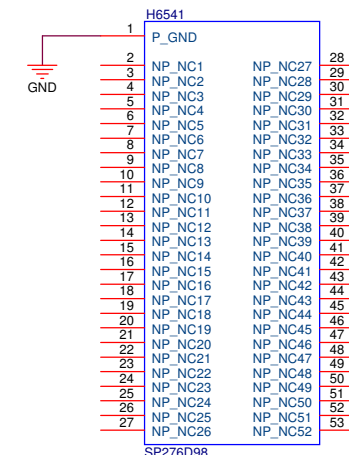
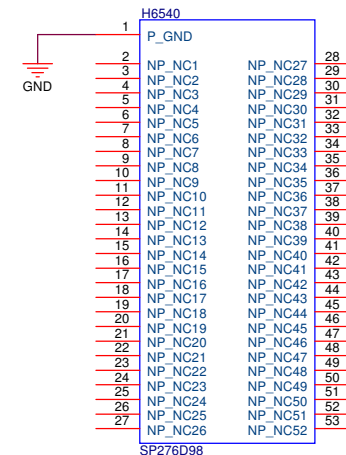
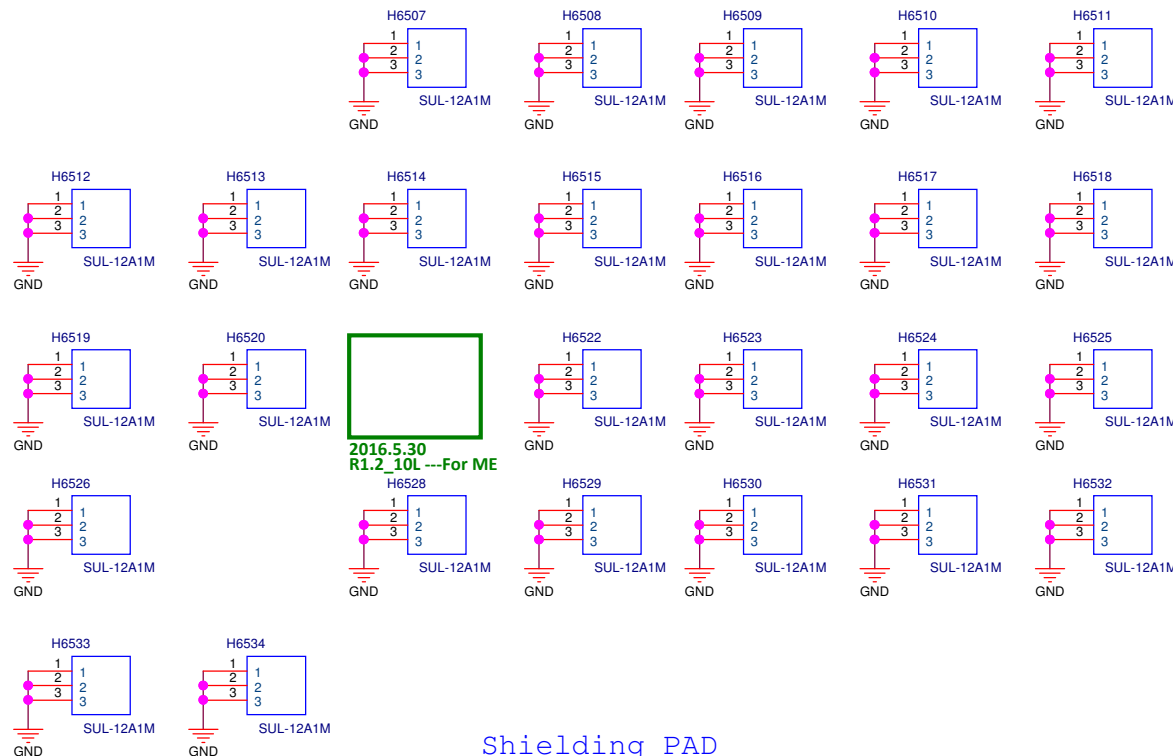
6\*3.1mm\*1



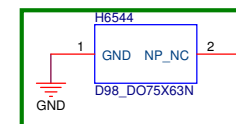
2016.6.6 R1.2\_10L ---For ME

# CLIP

Thermal screw\*2

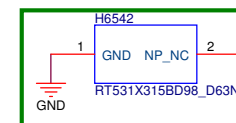


14\*8mm\*1



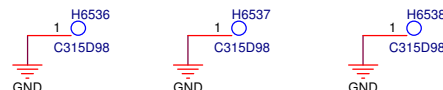
2016.6.6 R1.2\_10L ---For ME

13.5\*8mm\*1

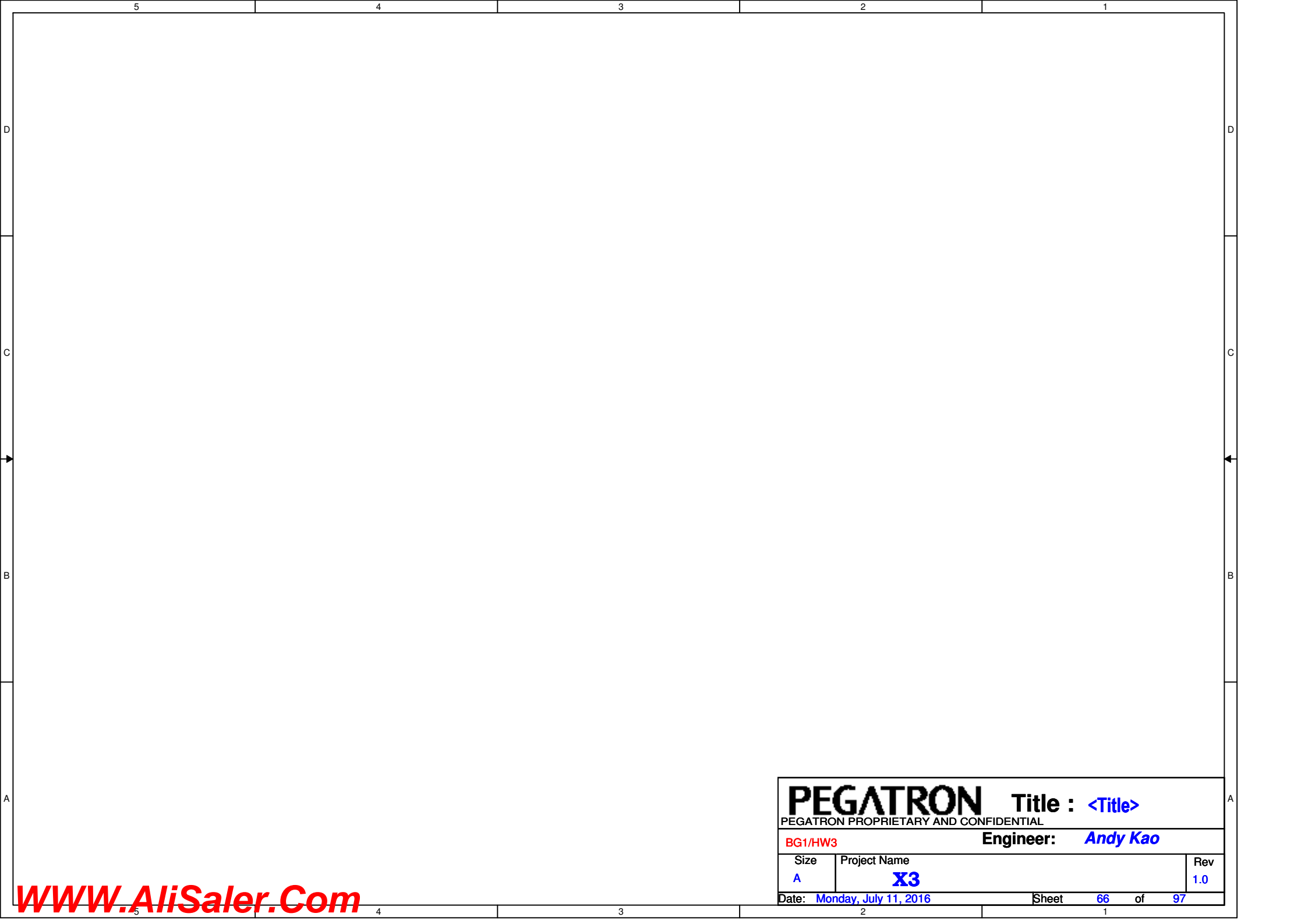


2016.6.6 R1.2\_10L ---For ME

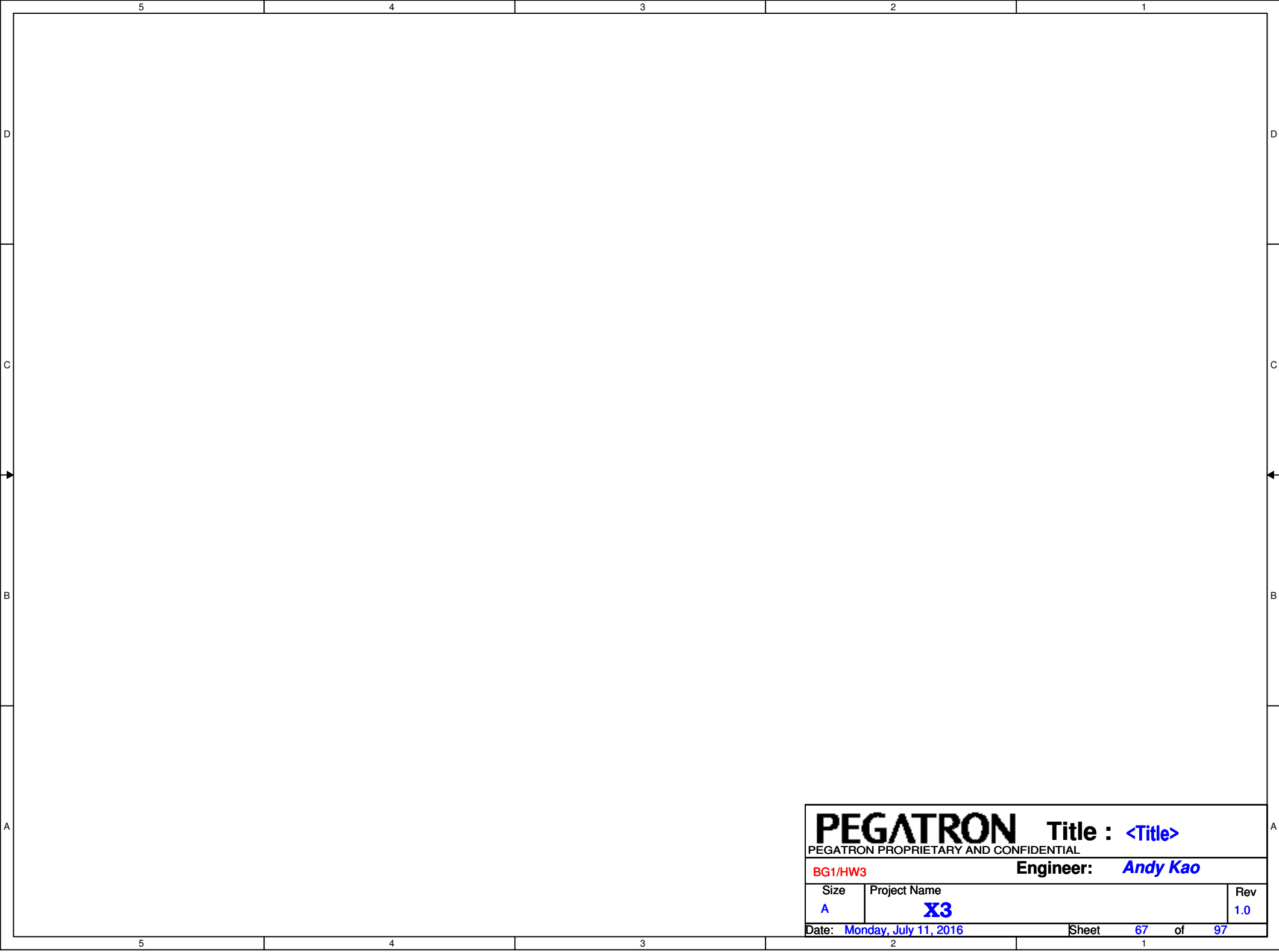
Shielding PAD



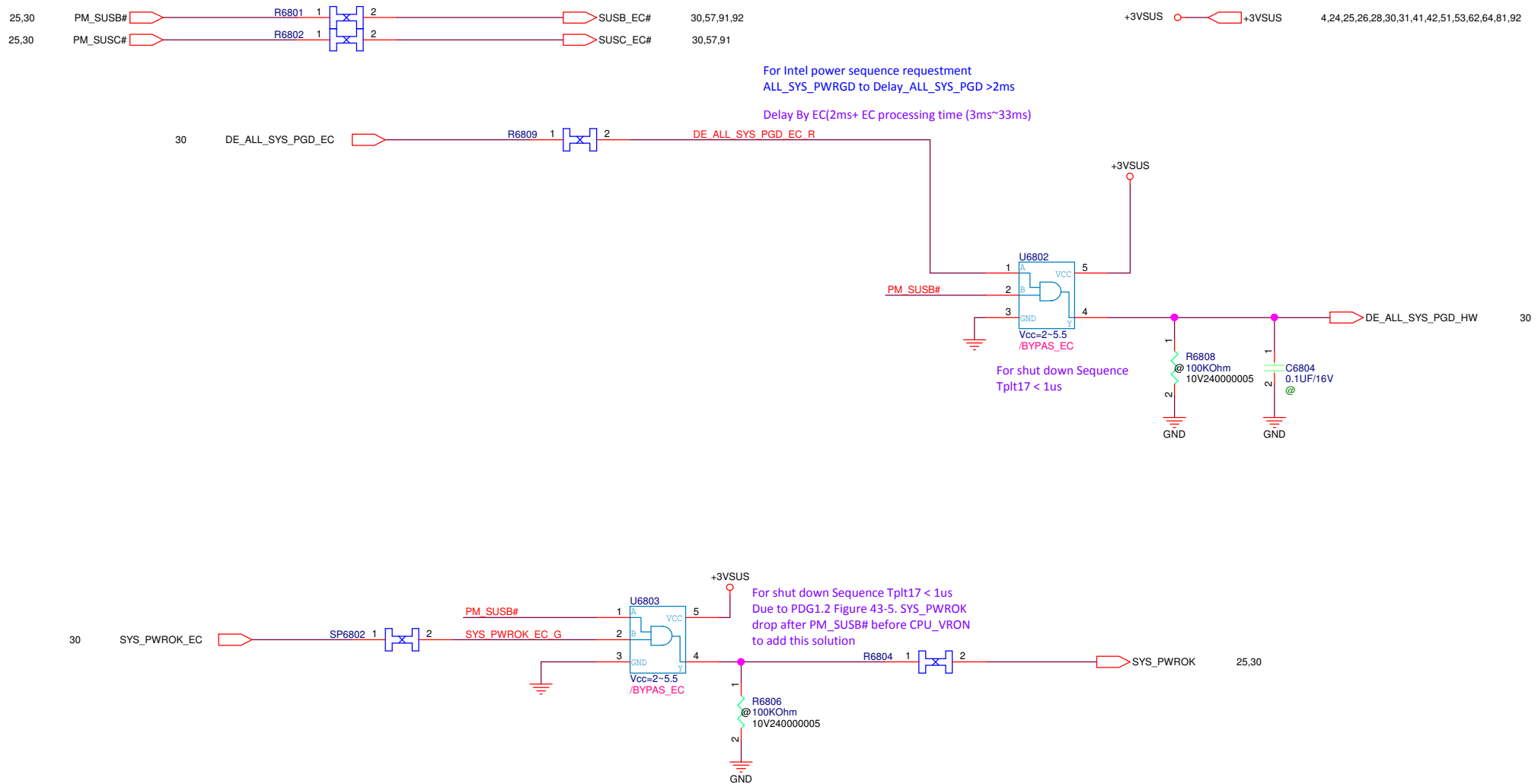
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3		Rev 1.0
Date: Monday, July 11, 2016		Sheet 65 of 97	



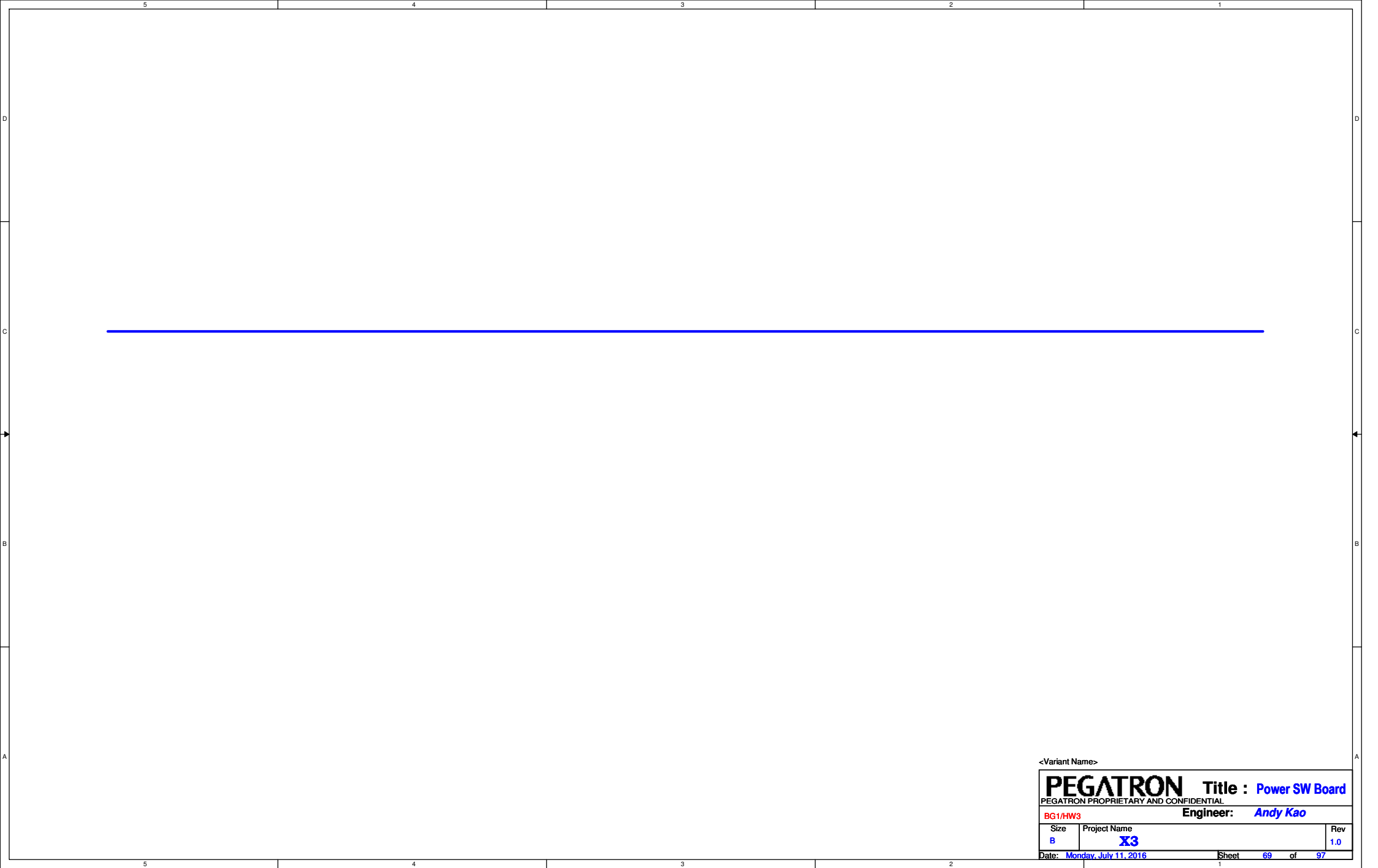
<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	66 of 97



<b>PEGATRON</b>		<b>Title :</b> <Title>
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>67</i> of <i>97</i>

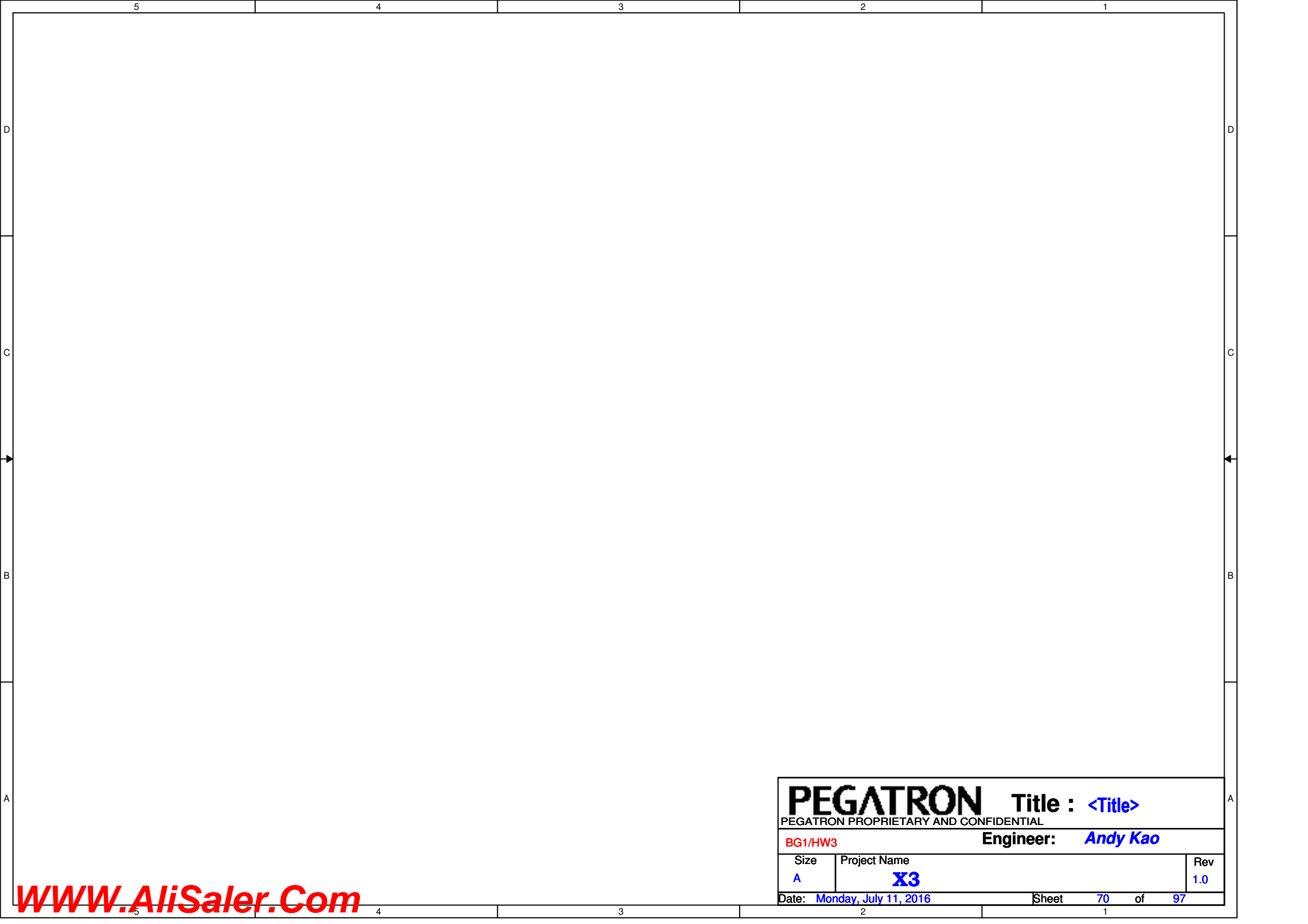


<b>PEGATRON</b>		Title : <b>POWER Sequence</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Andy Kao</b>	
Size <b>B</b>	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>68</b> of <b>97</b>	

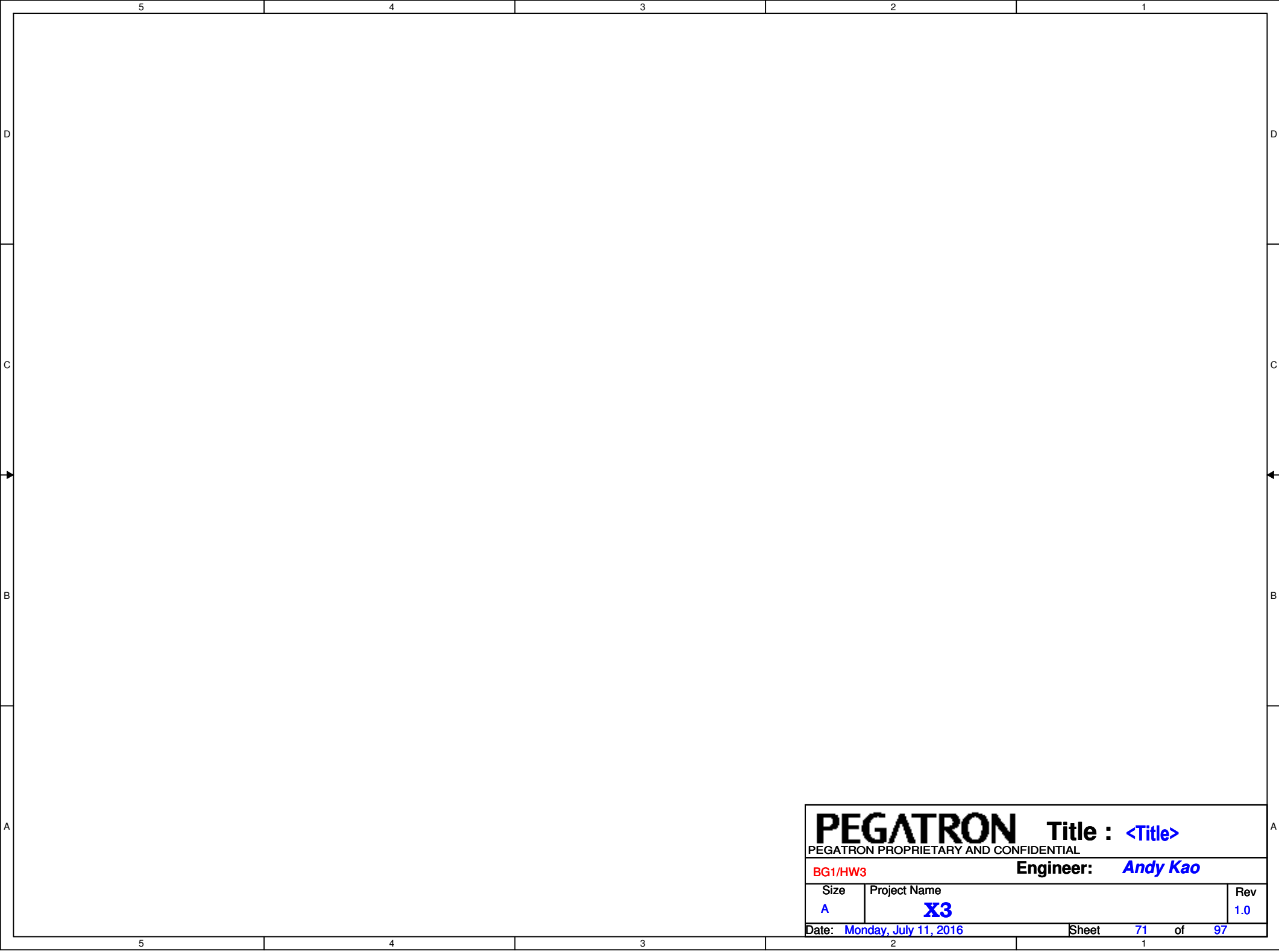


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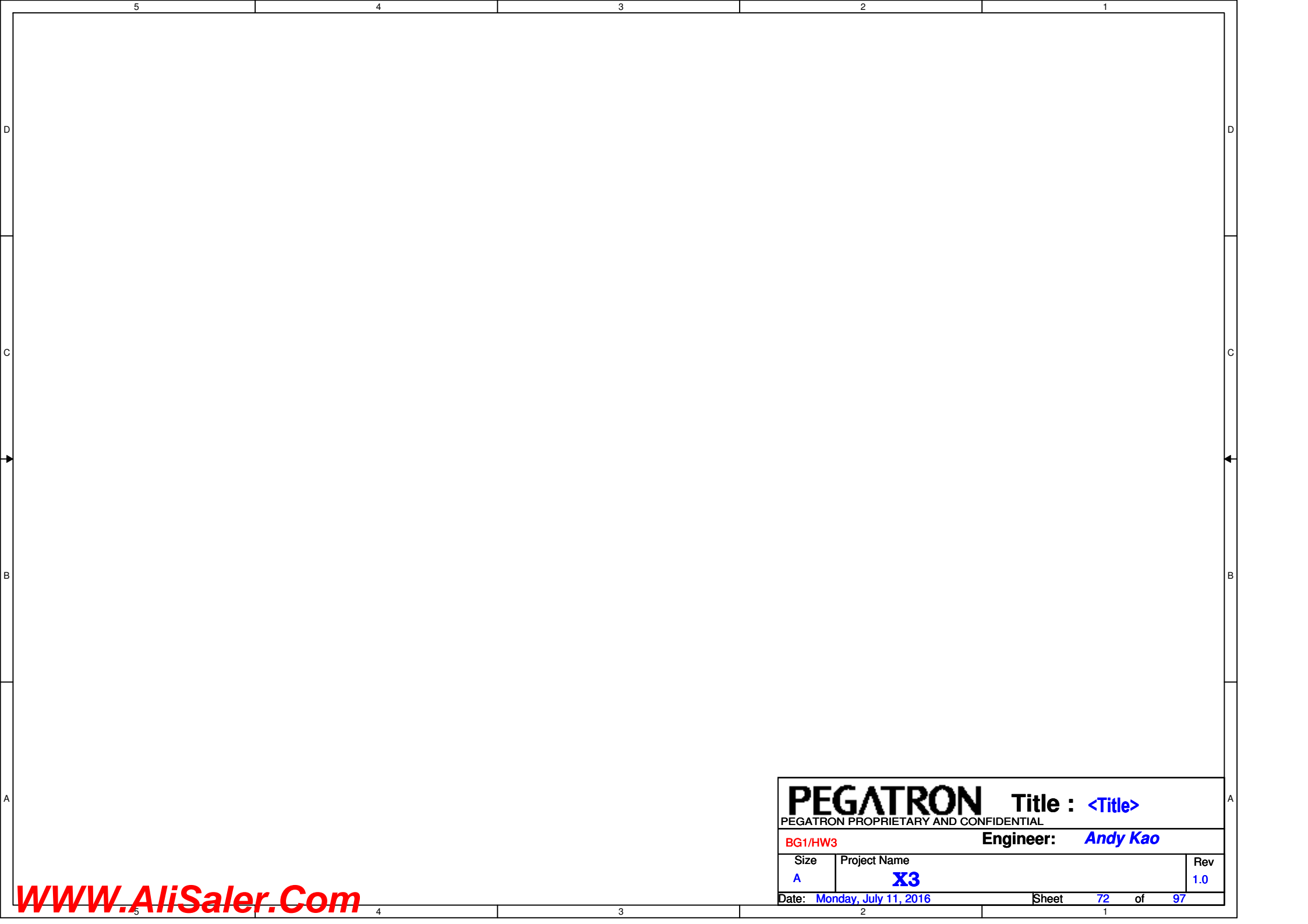
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> Andy Kao	
Size B	Project Name <b>X3</b>		Rev 1.0
Date: Monday, July 11, 2016		Sheet	69 of 97



<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	70 of 97

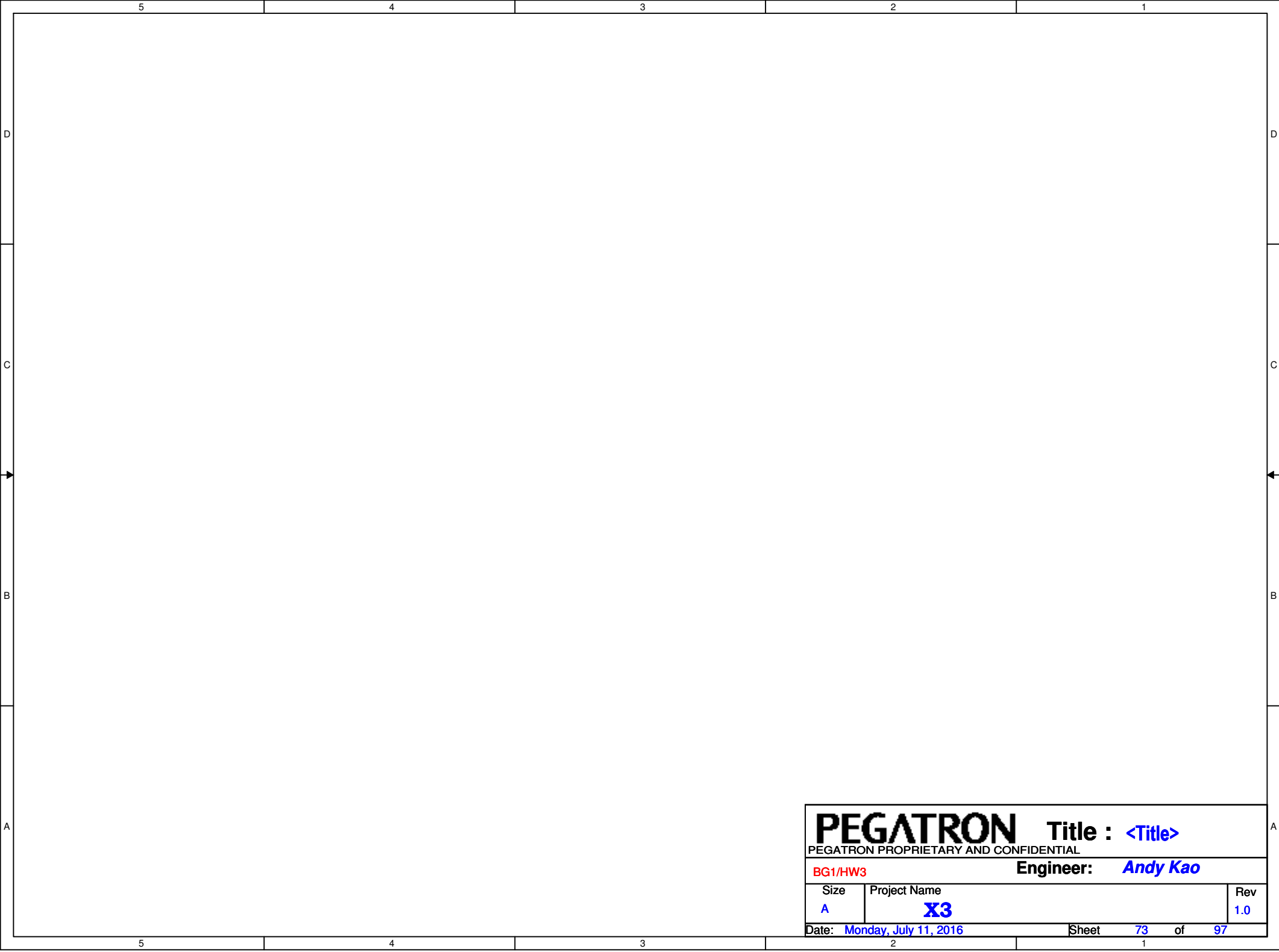


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>71</i> of <i>97</i>

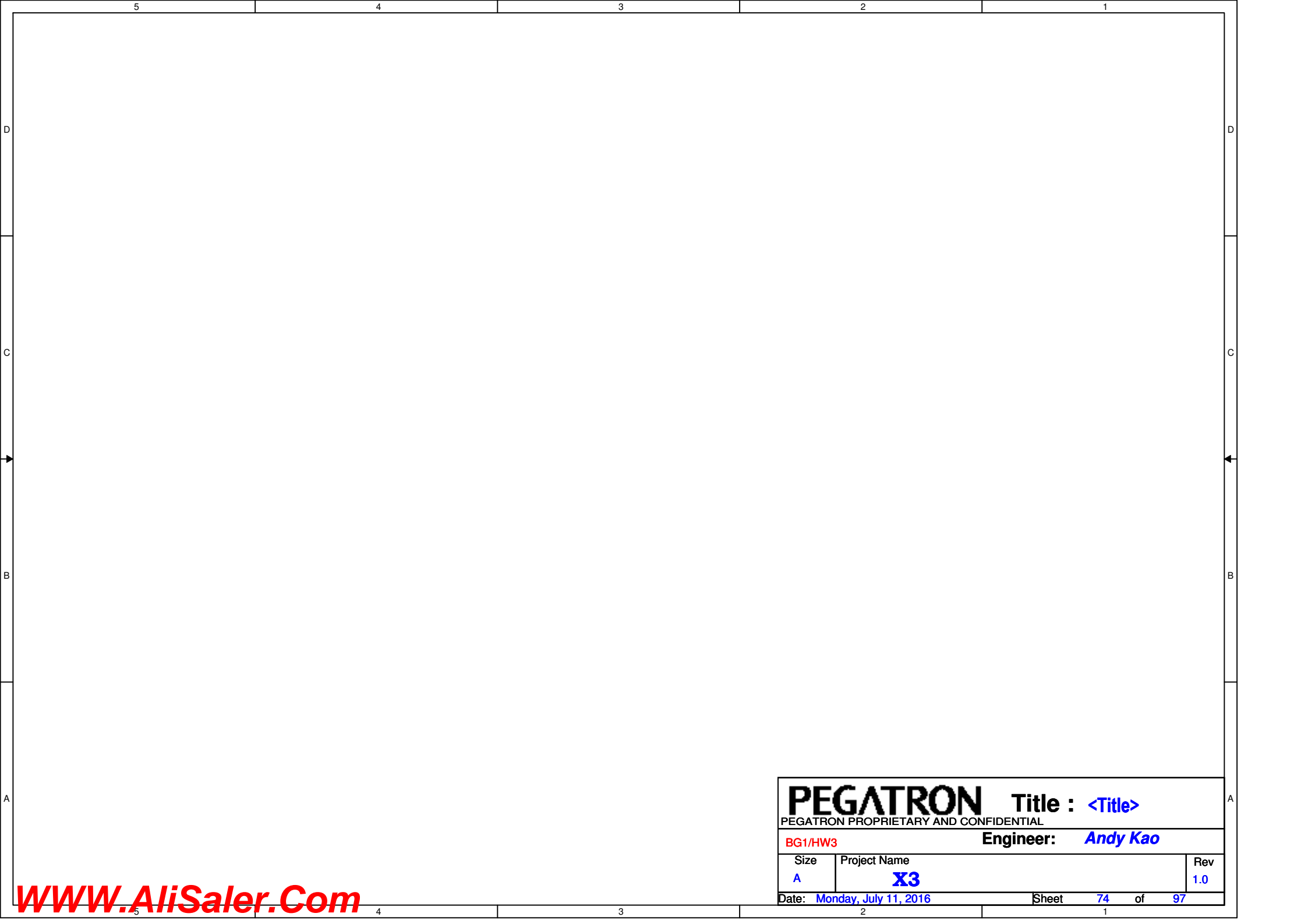


<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	72 of 97



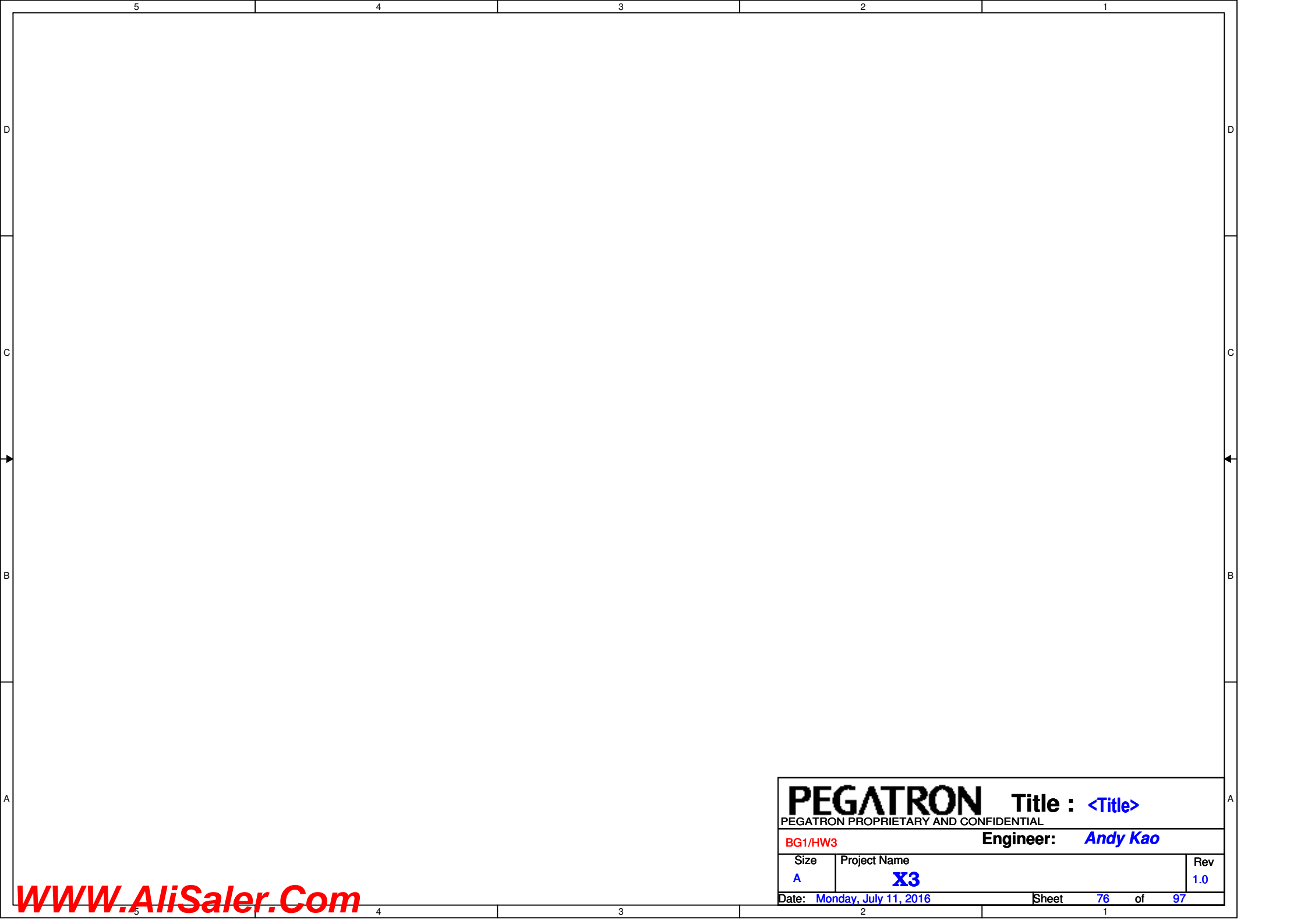


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Monday, July 11, 2016</b>		Sheet <b>73</b> of <b>97</b>

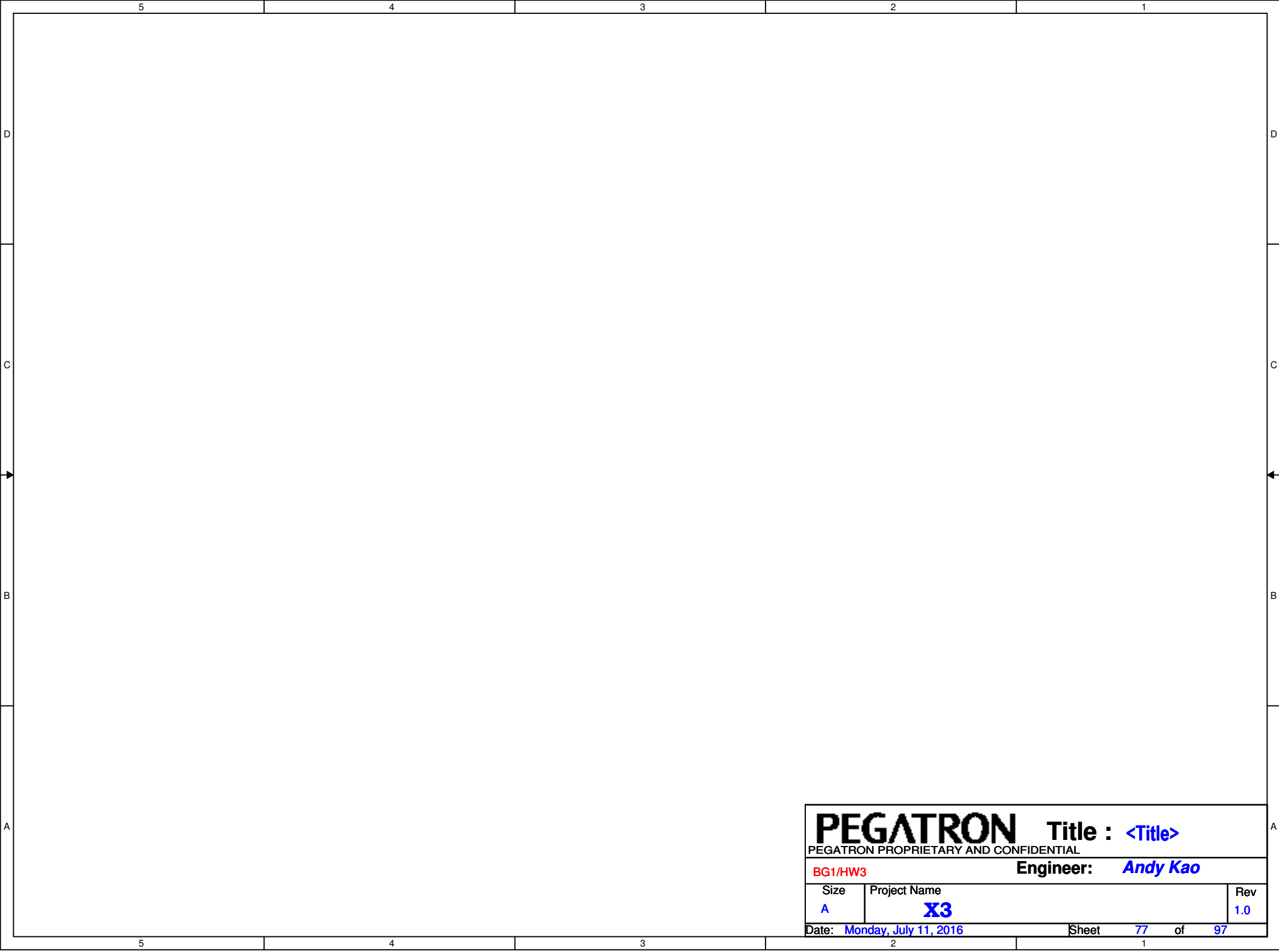


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>74</i> of <i>97</i>

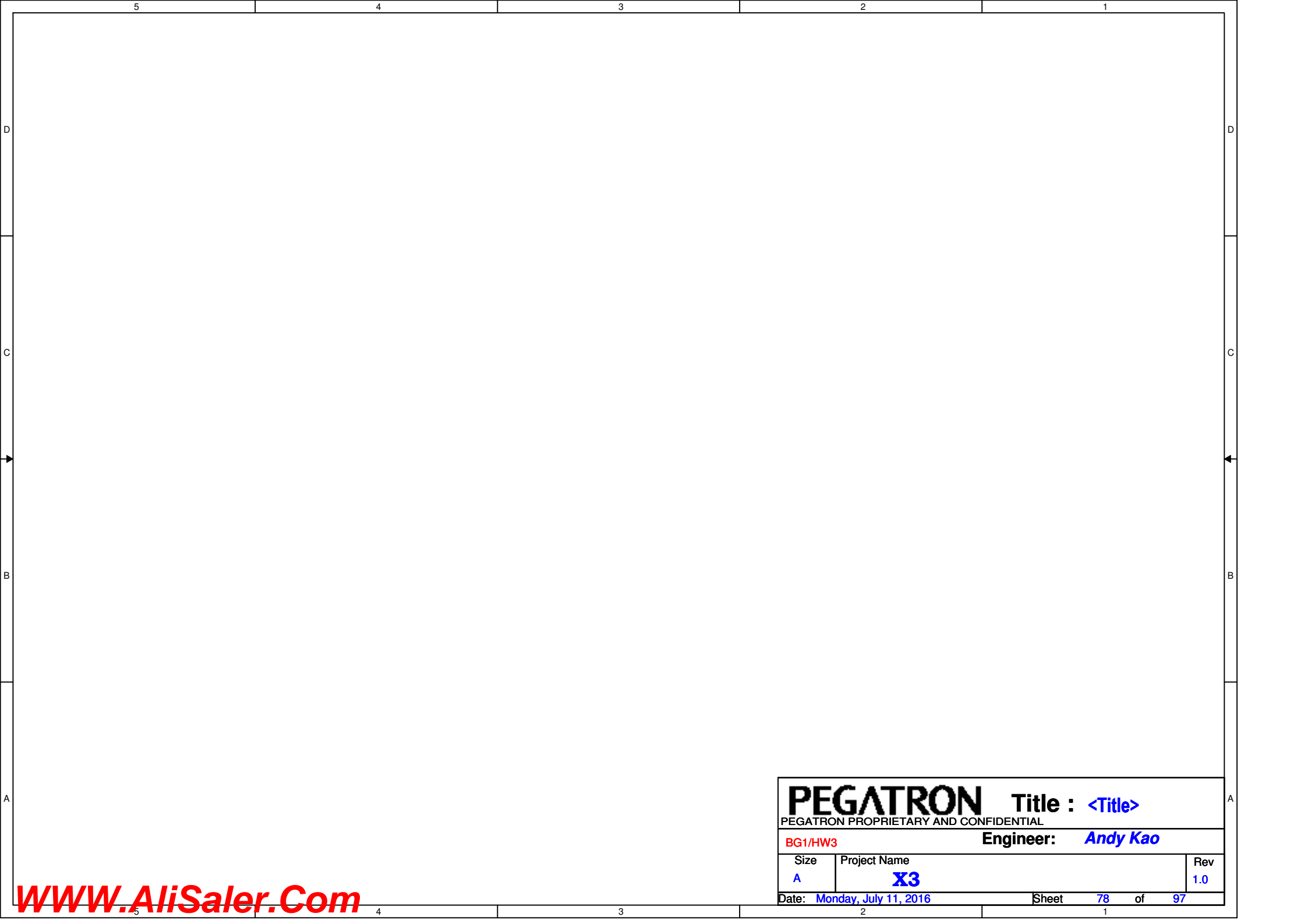
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<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>76</i> of <i>97</i>



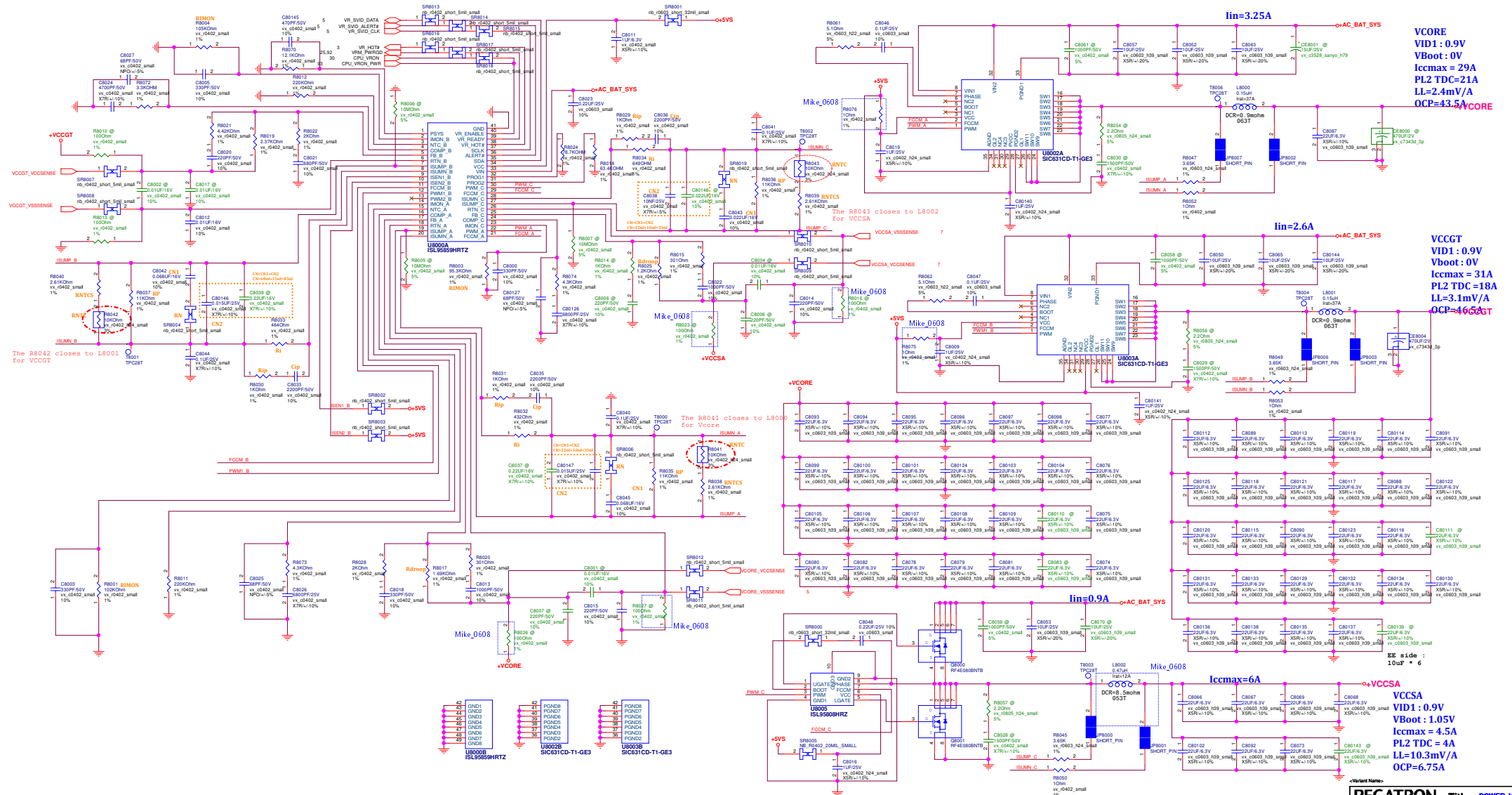
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <b>X3</b>		Rev <i>1.0</i>
Date: <i>Monday, July 11, 2016</i>		Sheet <i>77</i> of <i>97</i>	



<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> <i>Andy Kao</i>	
Size	Project Name		Rev
A	X3		1.0
Date: Monday, July 11, 2016		Sheet	78 of 97

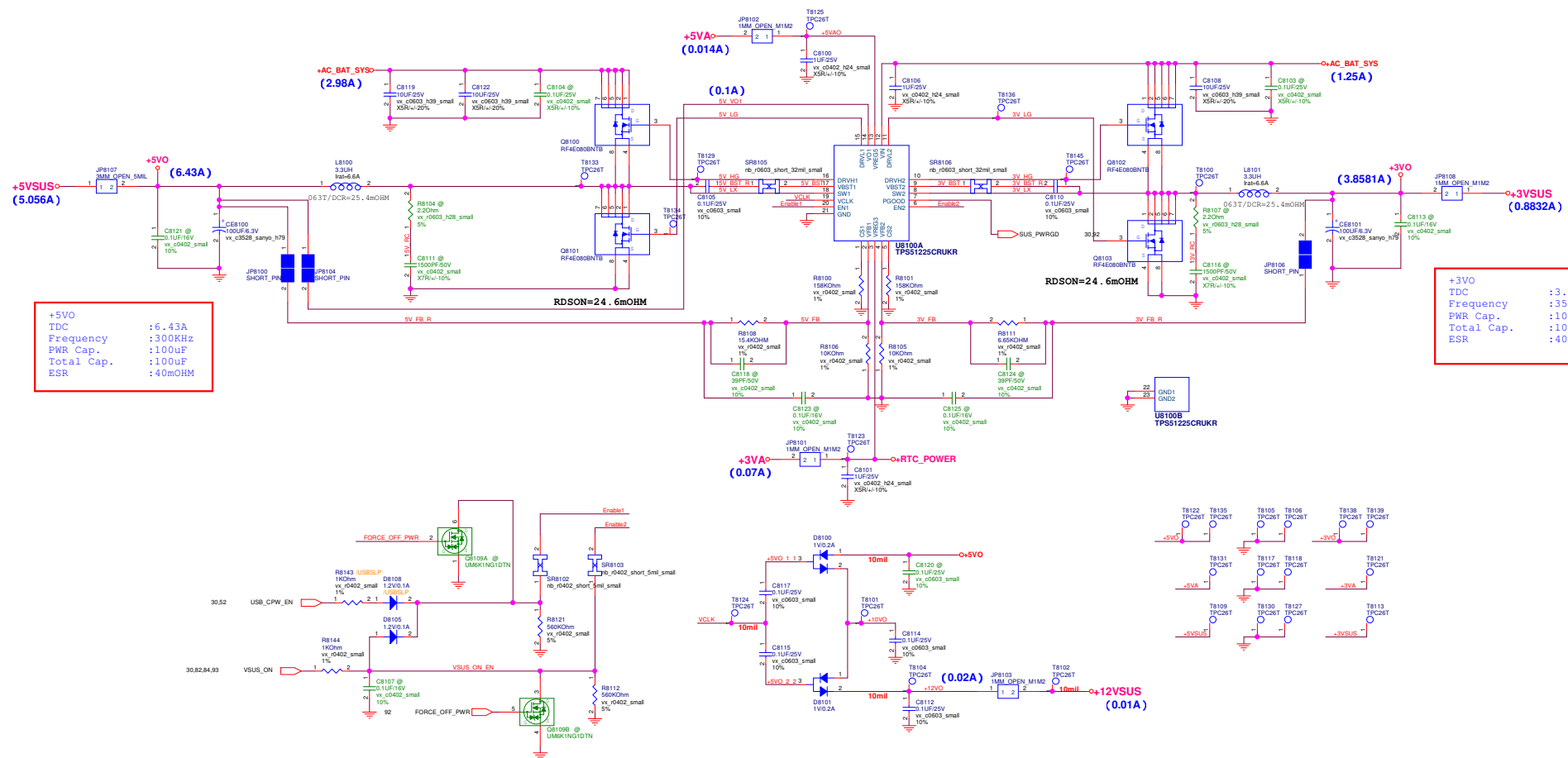
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# VCORE & VCCGT & VCCSA POWER SUPPLY

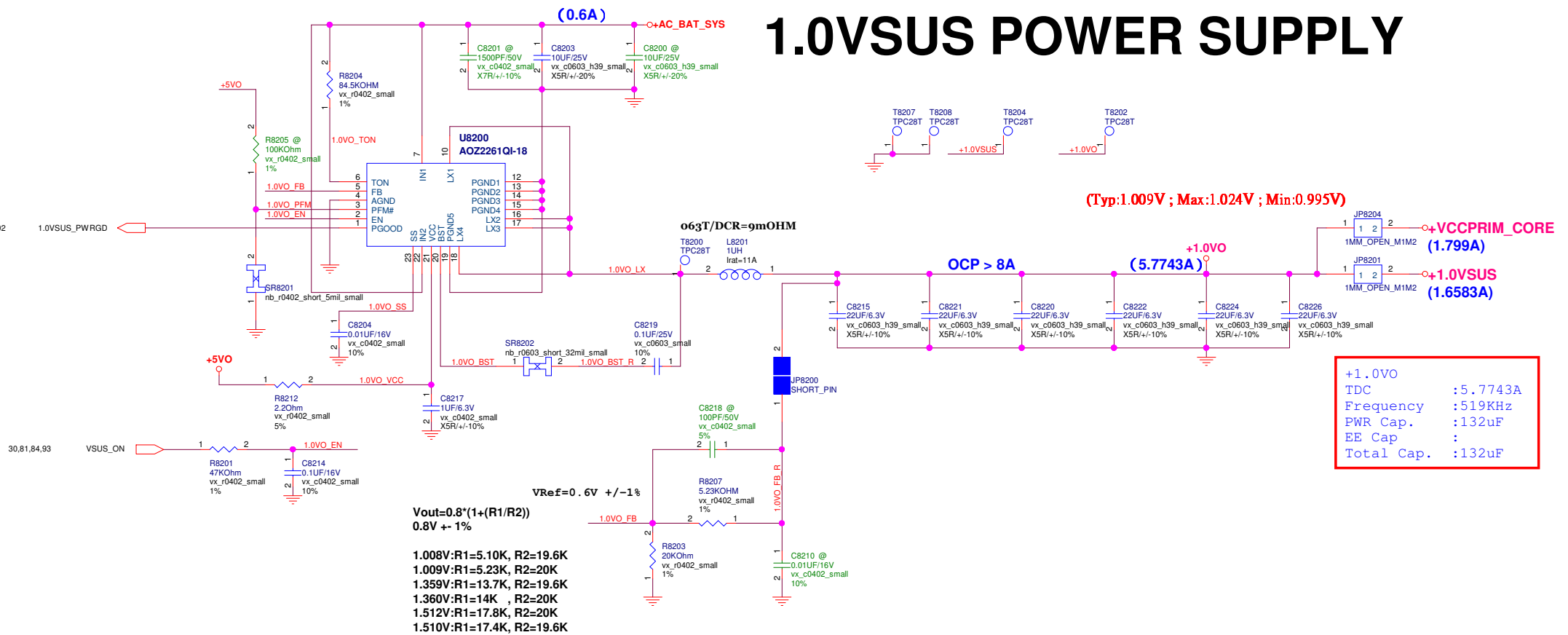




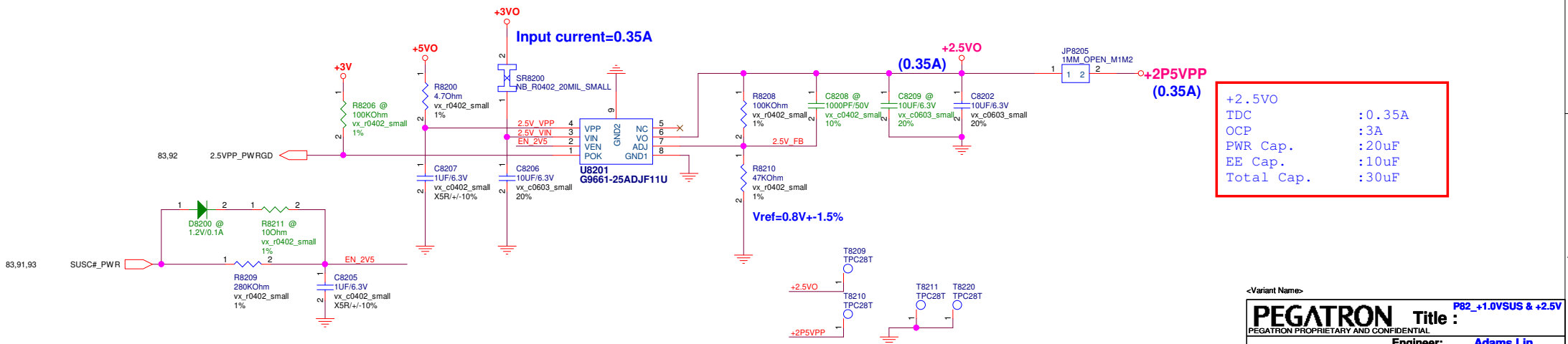
## 5VO & 3VO POWER SUPPLY



## 1.0VSUS POWER SUPPLY



## 2.5V POWER SUPPLY



# DDR & VTT POWER SUPPLY

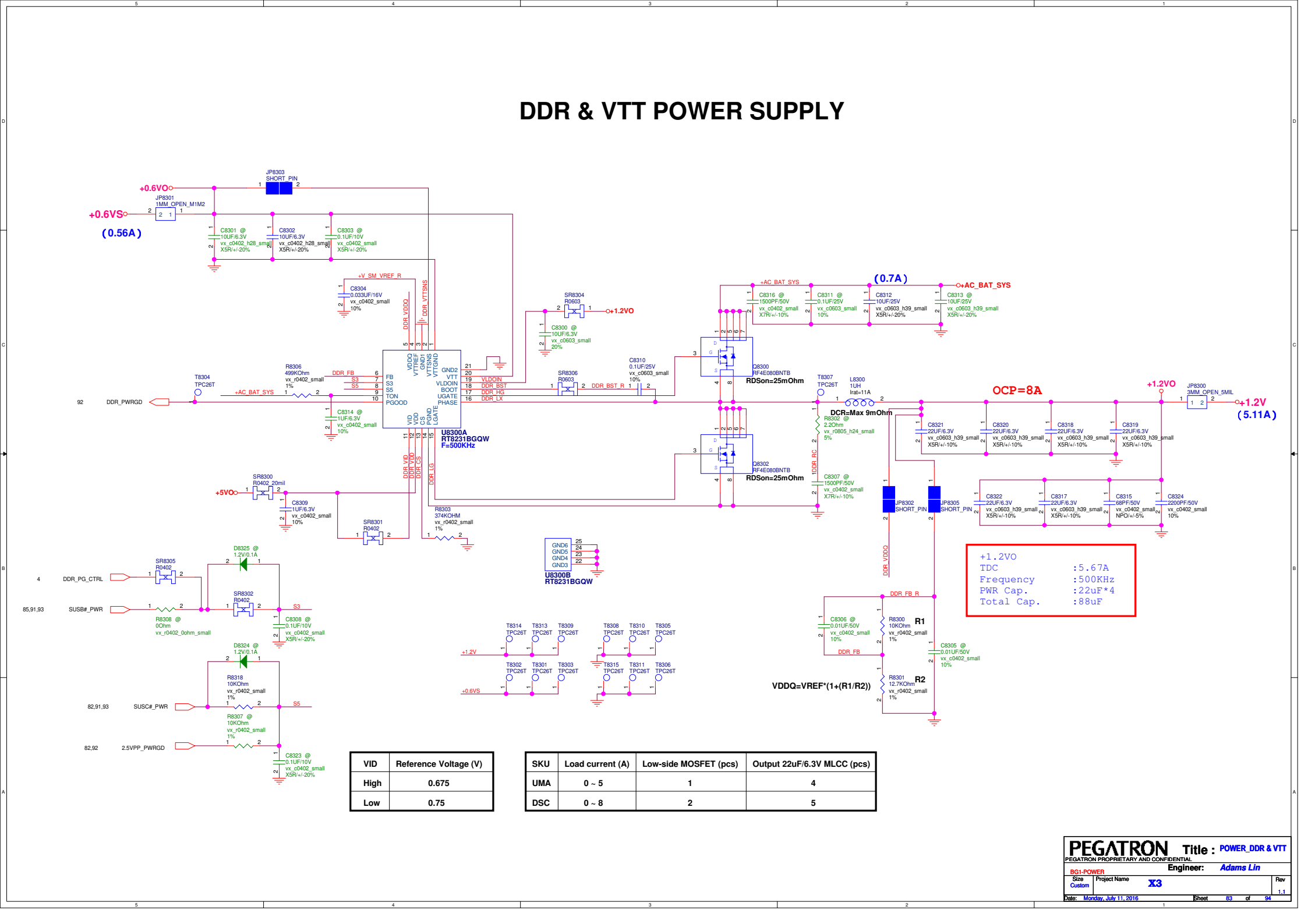
**VID Reference Voltage (V)**

VID	Reference Voltage (V)
High	0.675
Low	0.75

**SKU Load current (A) Low-side MOSFET (pcs) Output 22uF/6.3V MLCC (pcs)**

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

**PEGATRON** Title : POWER\_DDR & VTT  
PEGATRON PROPRIETARY AND CONFIDENTIAL  
BG1-POWER Engineer: Adams Lin  
Size Project Name X3 Rev  
Custom 1.1  
Date: Monday, July 11, 2016 Sheet 83 of 94



# DDR & VTT POWER SUPPLY

**VID Reference Voltage (V)**

VID	Reference Voltage (V)
High	0.675
Low	0.75

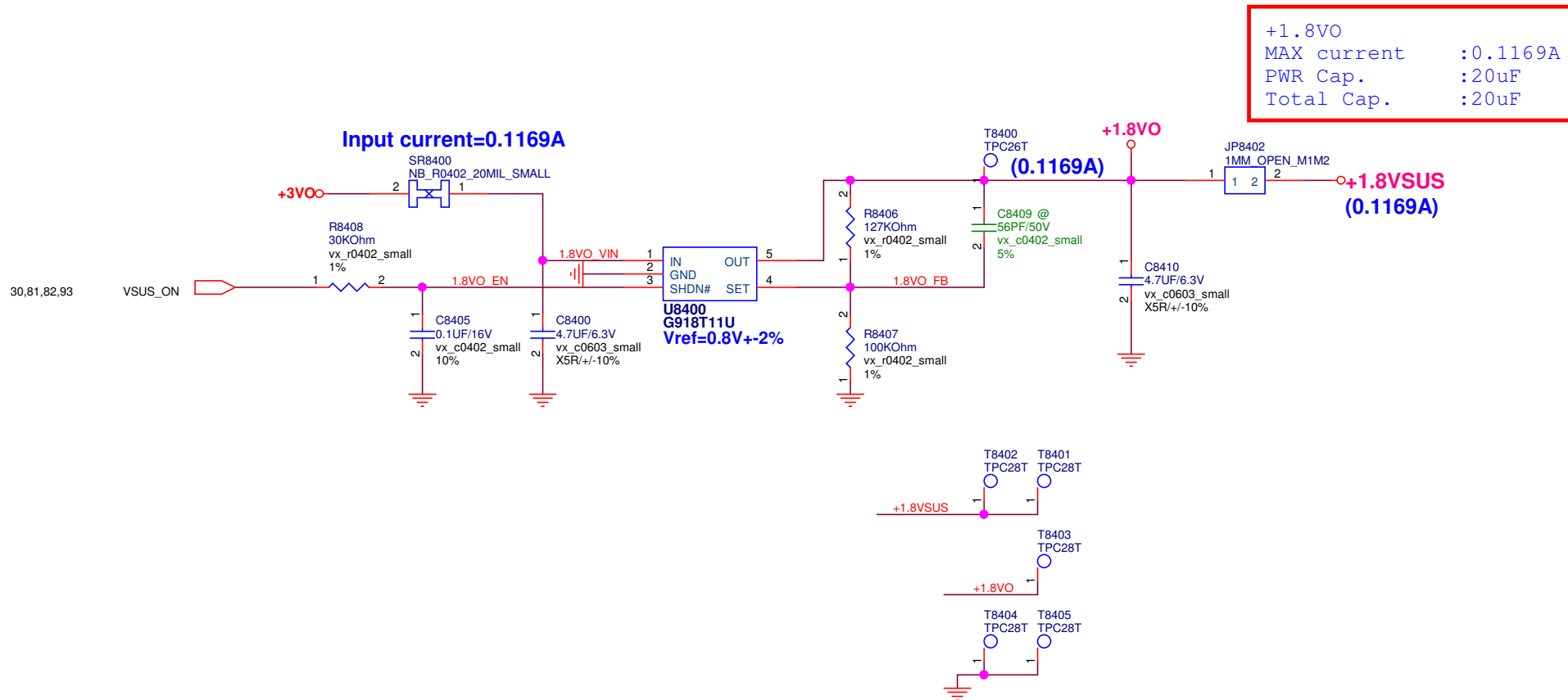
**SKU Load current (A) Low-side MOSFET (pcs) Output 22uF/6.3V MLCC (pcs)**

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

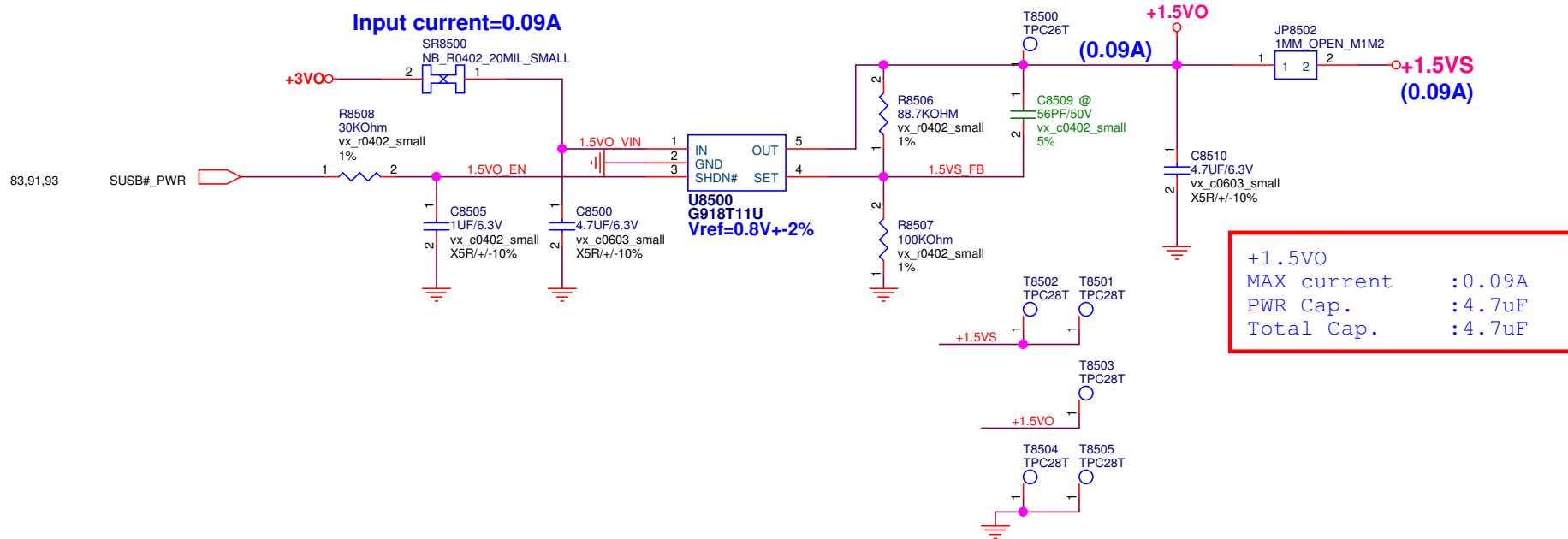
**PEGATRON** Title : POWER\_DDR & VTT  
PEGATRON PROPRIETARY AND CONFIDENTIAL  
BG1-POWER Engineer: Adams Lin  
Size Project Name X3 Rev  
Custom 1.1  
Date: Monday, July 11, 2016 Sheet 83 of 94

# DDR & VTT POWER SUPPLY

## 1.8VSUS POWER SUPPLY



## 1.5VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER\_+1.5VS

**Engineer:** **Adams Lin**

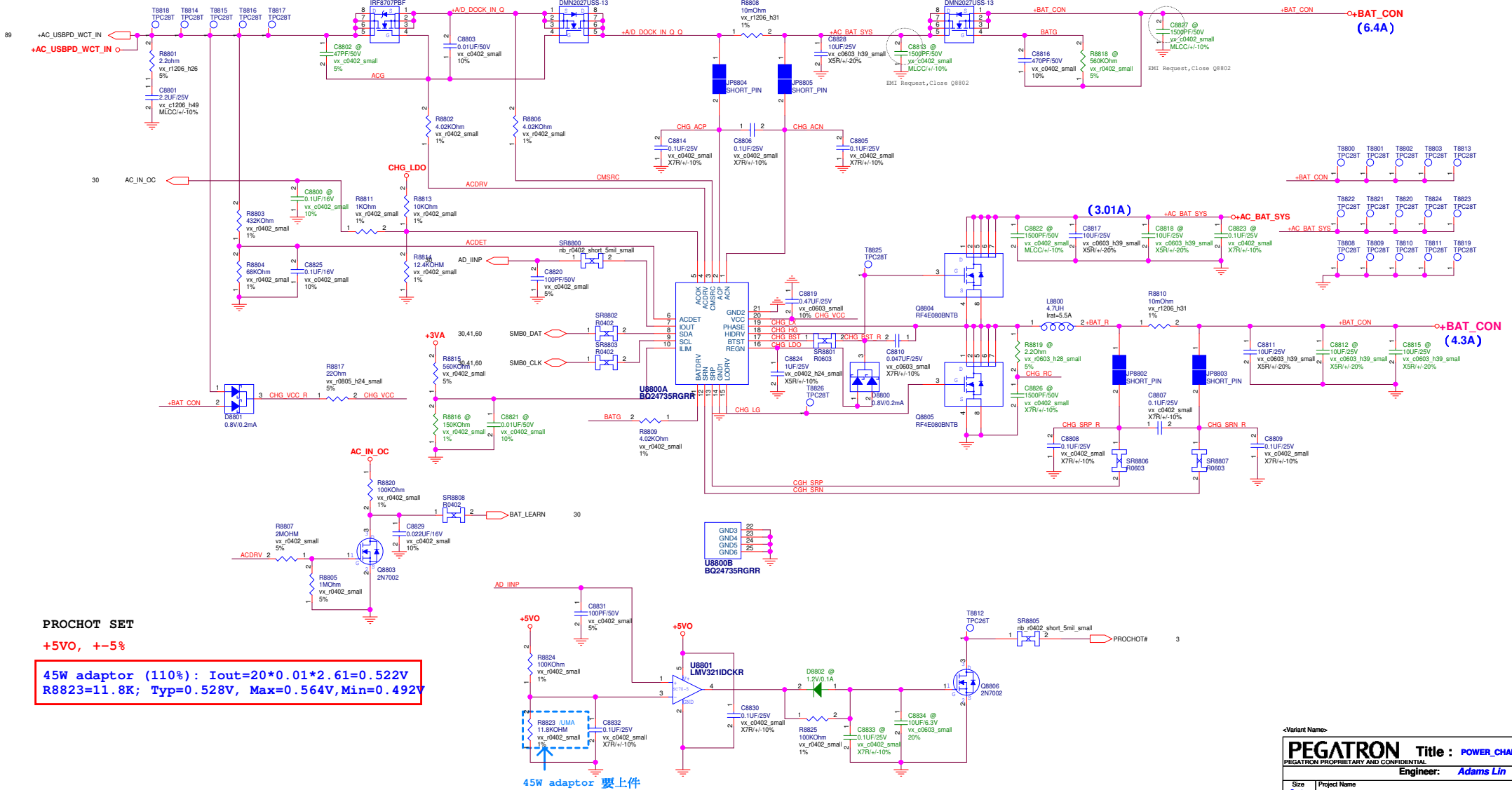
Size Custom	Project Name <b>Y3</b>	Rev
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Date: Monday, July 11, 2016

Sheet 85 of 94

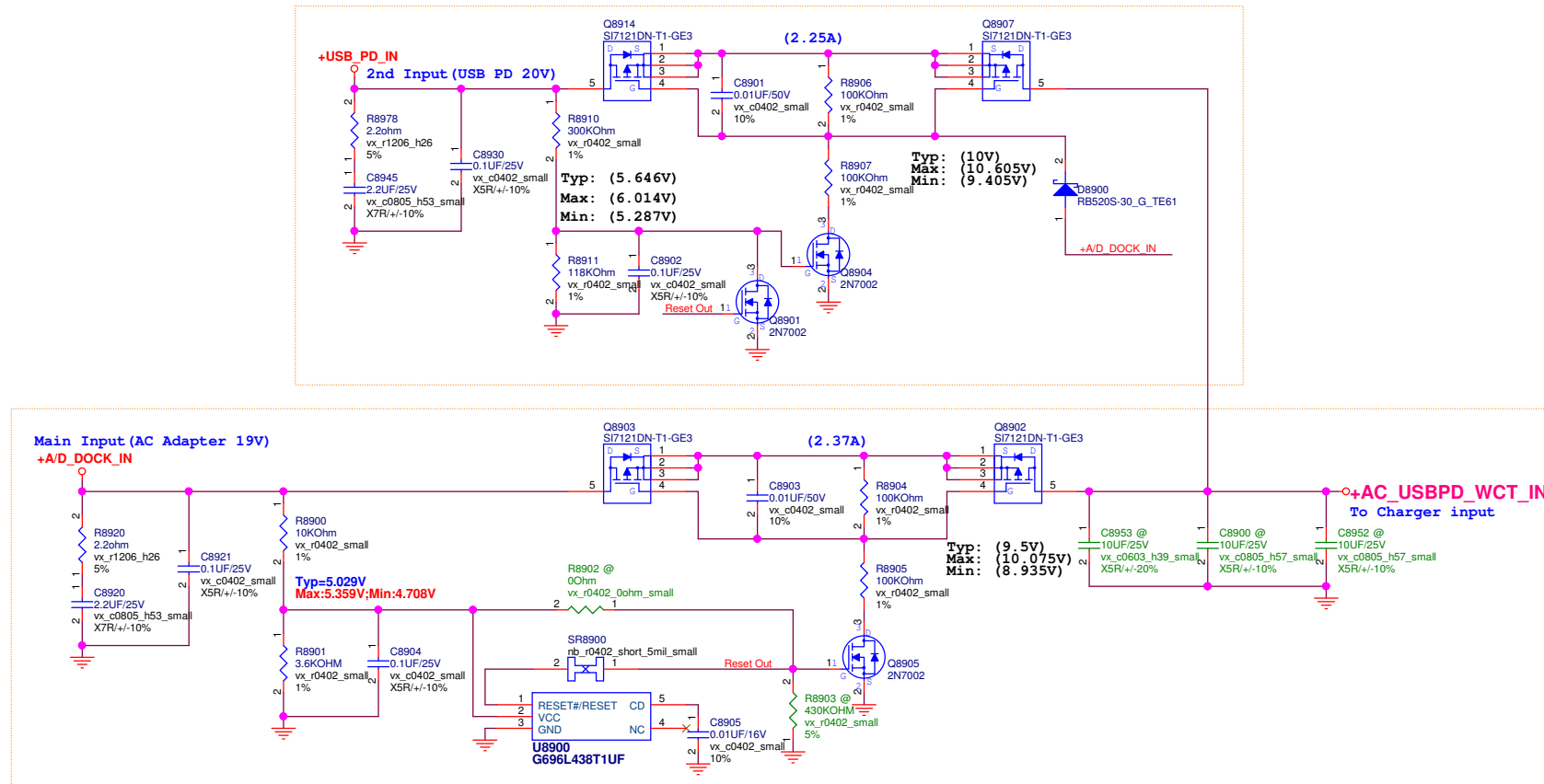
# BATTERY CHARGER

Adapter 65W=3.42A  
Adapter 45W=2.37A

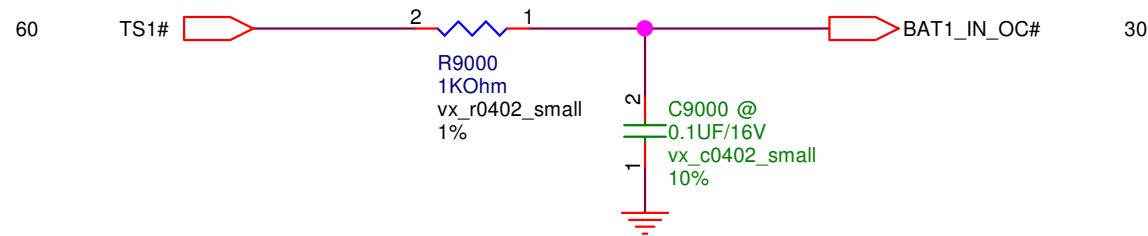


Pegatron Title : POWER_CHARGER	
Pegatron PROPRIETARY AND CONFIDENTIAL	
Engineer: Adams Lin	
Size	Project Name
Custom	X3
Date: Monday, July 11, 2016	Sheet 66 of 64

## 2 Input switch Circuit



## BATTERY IN DETECT



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_DETECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Adams Lin</b>	
Size <b>Custom</b>	Project Name <b>X3</b>		Rev <b>1.1</b>
Date:	<b>Monday, July 11, 2016</b>	Sheet	<b>90</b> of <b>94</b>



[illegible]

**(2.184A)**

VGS = 10V , RDSon = 5.1mOHM

Q9104  
SISA14DN-T1-GE3

C9120 @  
0.1UF/6.3V  
vx\_c0402\_small  
X5R/+/ -10%

C9134 @  
0.033UF/16V  
vx\_c0402\_small  
10%

R9107  
22KOhm  
vx\_r0402\_small  
1%

T9111  
TPC26T

C9135  
0.1UF/16V  
vx\_c0402\_small  
10%

C9160 @  
0.1UF/16V  
vx\_c0402\_small  
10%

C9136 @  
22UF/6.3V  
vx\_c0603\_h39\_small  
X5R/+/ -10%

**+VCCIO  
(2.184A)**

**VGS=10V, RDSon=27.6mOHM**

Q9102  
SSM3K315T

**+5V (1.29A)**

C9103  
0.033UF/16V  
vx\_c0402\_small  
10%

R9102  
4.7KOhm  
vx\_r0402\_small  
1%

T9107  
TPC26T

C9114  
0.1UF/16V  
vx\_c0402\_small  
10%

**+5VS (1.29A)**

**+12VSUS**

**10mil**

SUS# PWR

Q9100

R9103  
560KOhm  
vx\_r0402\_small  
5%

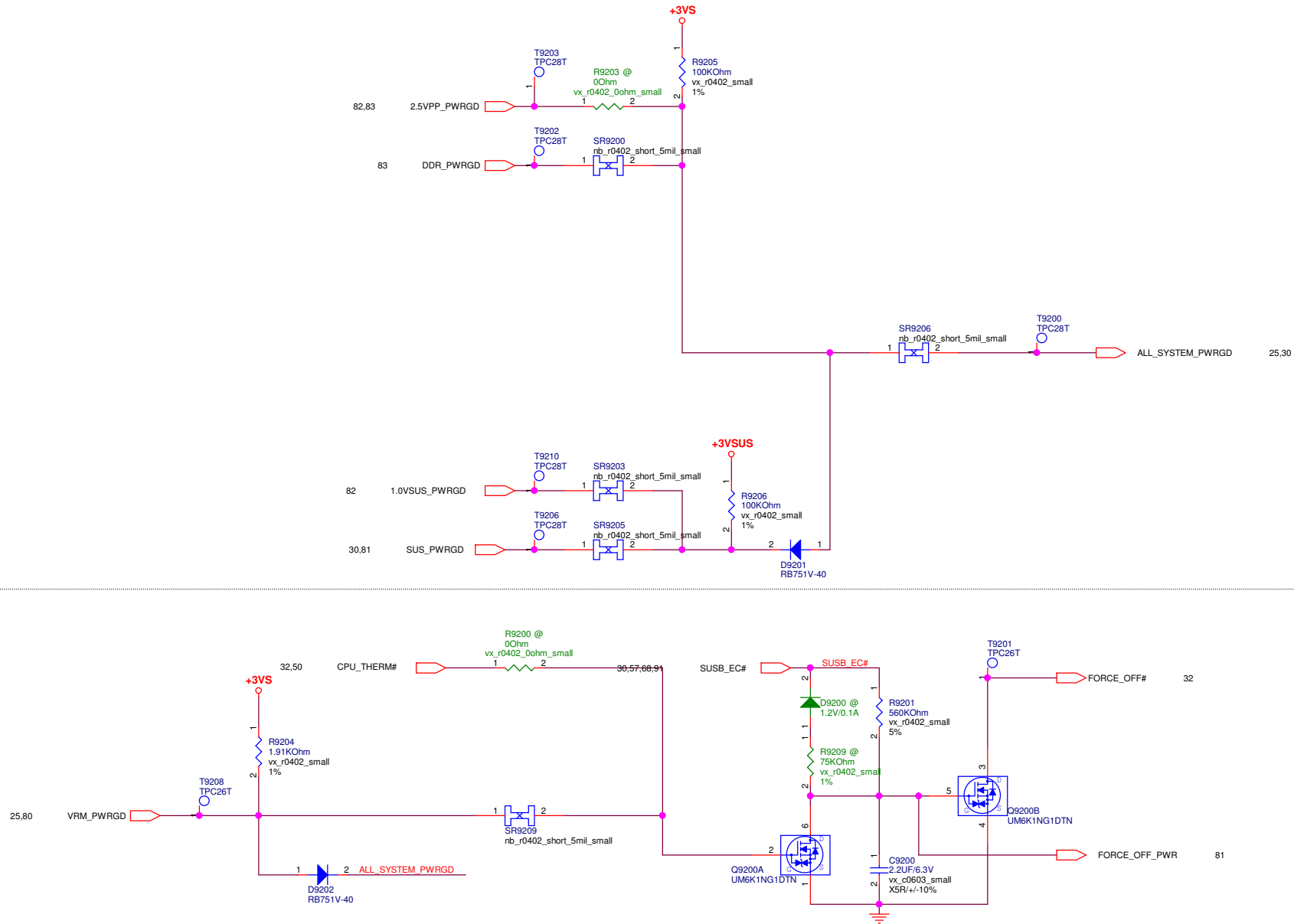
T9105  
TPC26T

**10mil**

**+12VS  
(0.005A)**

[illegible]

# POWER GOOD DETECTOR

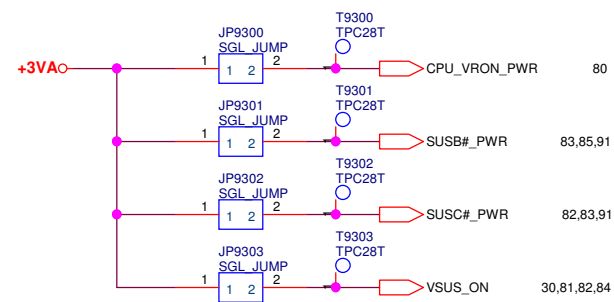


<Variant Name>

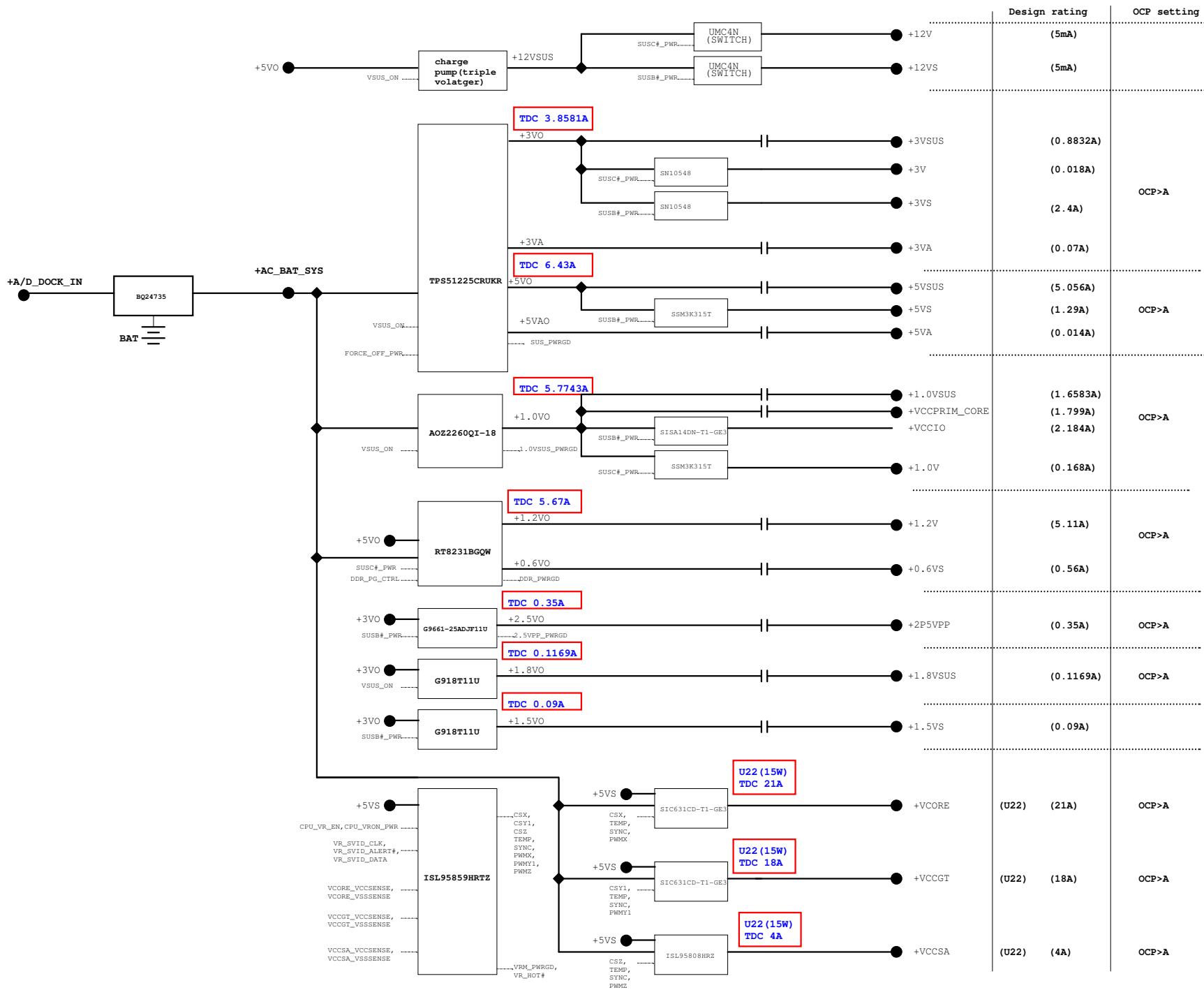
<b>PEGATRON</b>		Title : <b>POWER_PROTECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		<b>Adams Lin</b>	
Size Custom	Project Name <b>X3</b>	Rev 1.1	
Date: <b>Monday, July 11, 2016</b>	Sheet <b>92</b> of <b>94</b>		

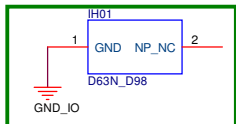
+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	→	+5VO	26,81,82,83,88,91
+3VO	→	+3VO	81,82,84,85,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.2VO	→	+1.2VO	83
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	28,81,91
+5VSUS	→	+5VSUS	41,42,52,56,64,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,22,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	57,91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,19,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	31,48,57,91
+5VS	→	+5VS	31,36,45,48,50,51,57,80,91
+3VS	→	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	→	+0.6VS	15,57,83
+VCORE	→	+VCORE	5,80
+VCCGT	→	+VCCGT	6,80
+VCCSA	→	+VCCSA	7,80
+VCCIO	→	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82

## FOR POWER TEST

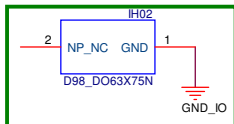


<b>PEGATRON</b>		<b>Title : POWER_SIGNAL</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1-POWER</b>		<b>Engineer: Adams Lin</b>	
Size <b>B</b>	Project Name <b>X3</b>	Rev <b>1.1</b>	
Date: <b>Monday, July 11, 2016</b>		Sheet <b>93</b> of <b>94</b>	



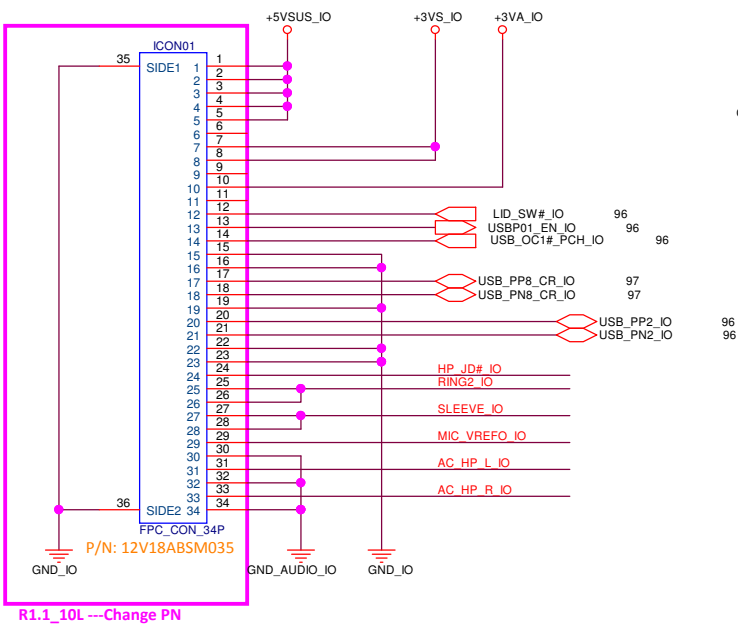
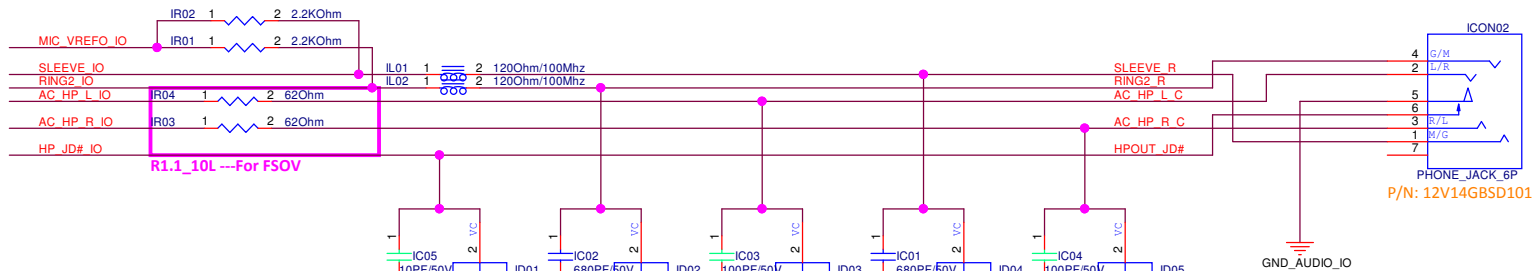


2016.6.6 R1.2\_10L ---For ME

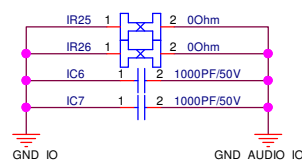


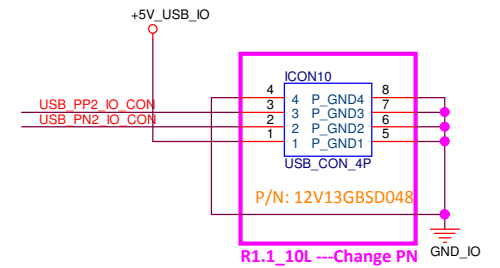
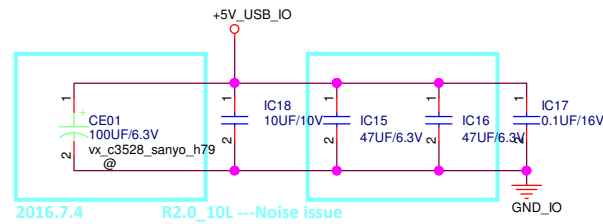
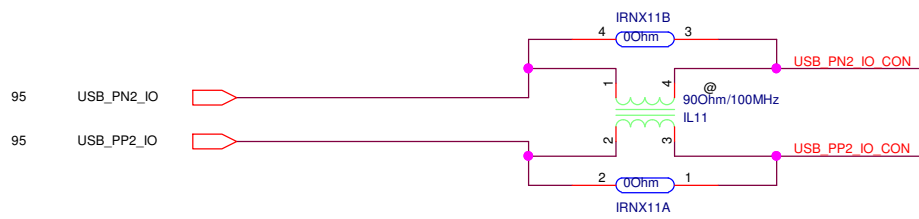
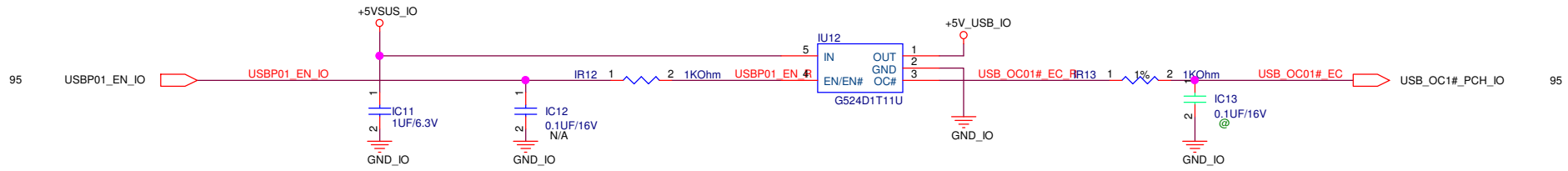
2016.6.6 R1.2\_10L ---For ME

## AUDIO JACK

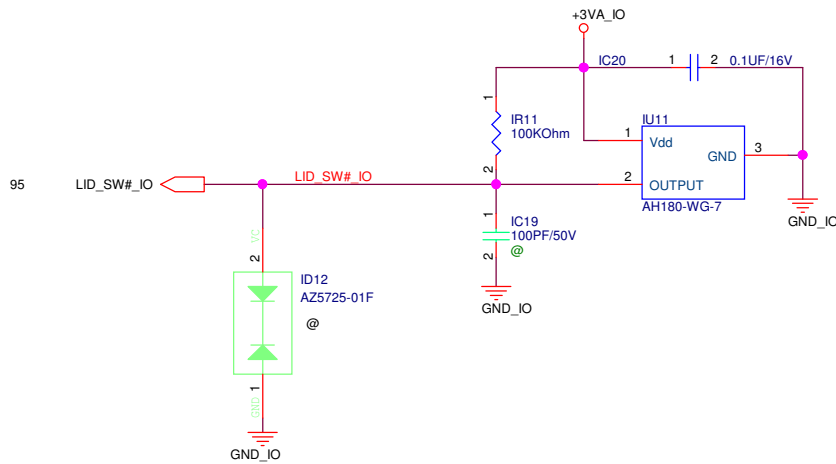
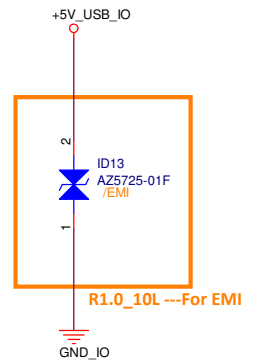
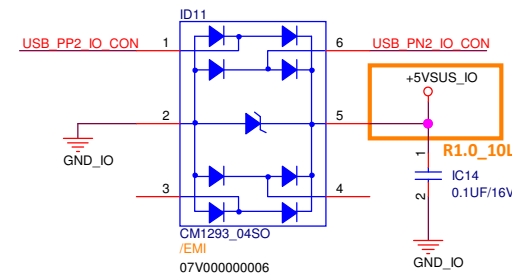


R1.1\_10L ---Change PN



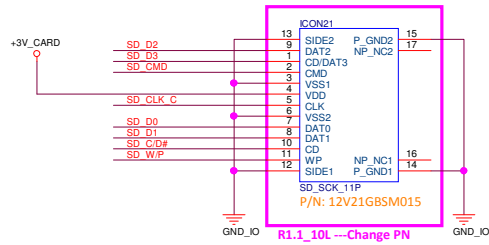
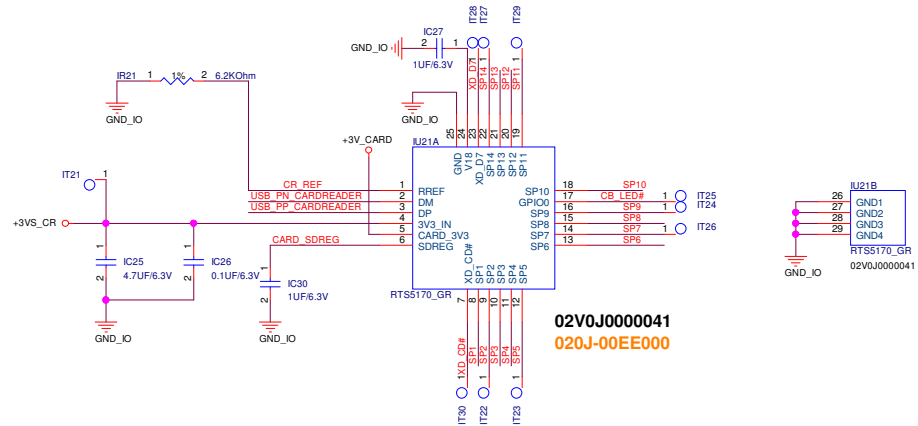
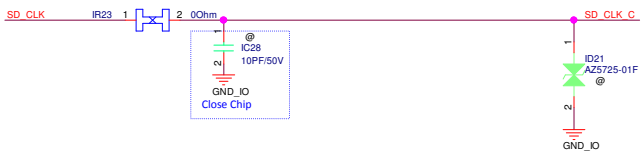
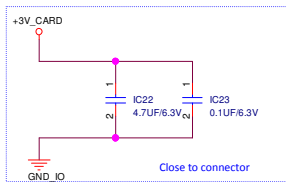
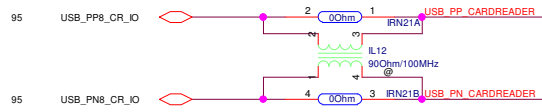
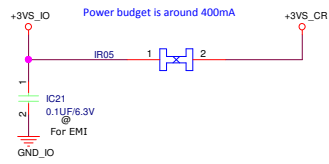


PLACE ESD Diodes near USB Connector



<b>PEGATRON</b>		<b>Title : USB30_IO_CONN</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size B	Project Name <b>X3</b>	Rev <b>1.0</b>	
Date: <b>Monday, July 11, 2016</b>		Sheet <b>96</b> of <b>97</b>	

# Cardreader



### RTS5170-GR Share Pin Assignment

SP1	SD_W/P
SP3	SD_D1
SP4	SD_D0
SP6	SD_C/D#
SP8	SD_CLK
SP10	SD_CMD
SP12	SD_D3
SP13	SD_D2